

PG141-H00

GA104/NP GB5/5B-256 DESIGN, 16GB GDDRx, 256b, X16 DP + DP + DP + HDMI/DP

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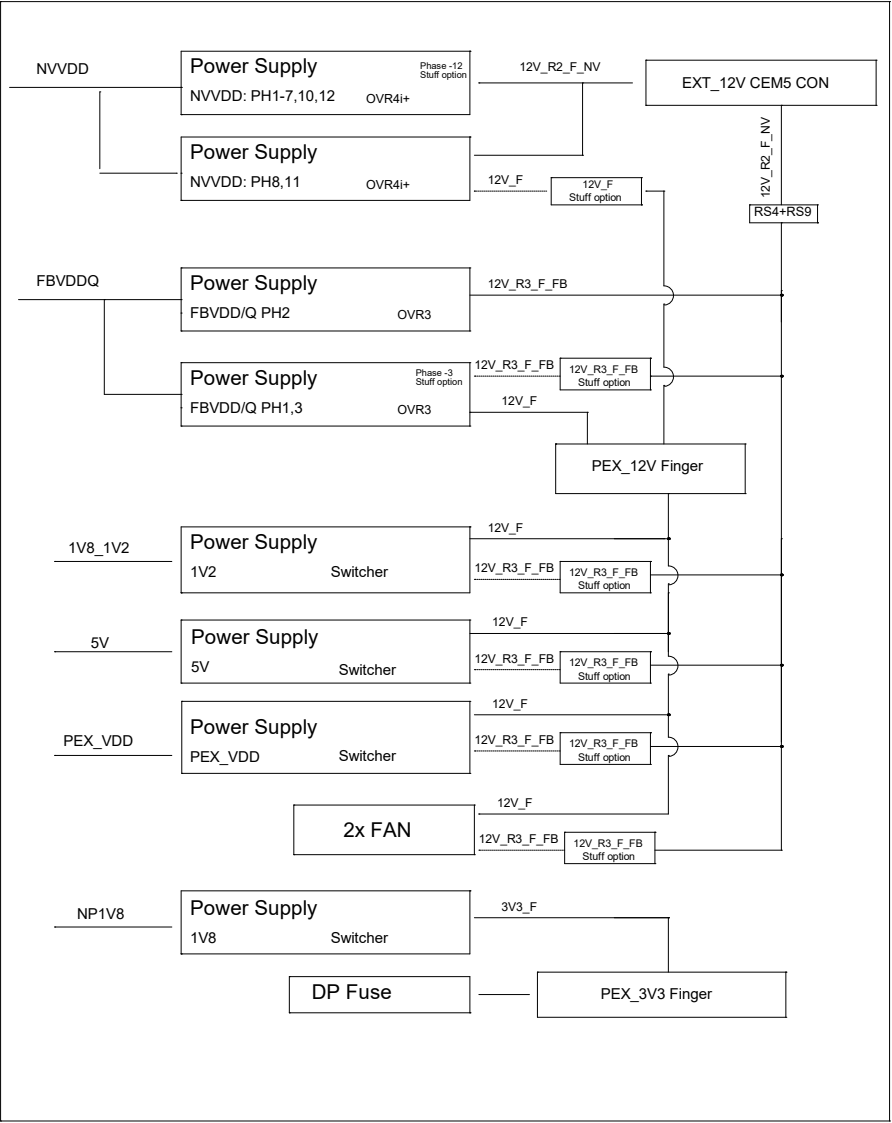
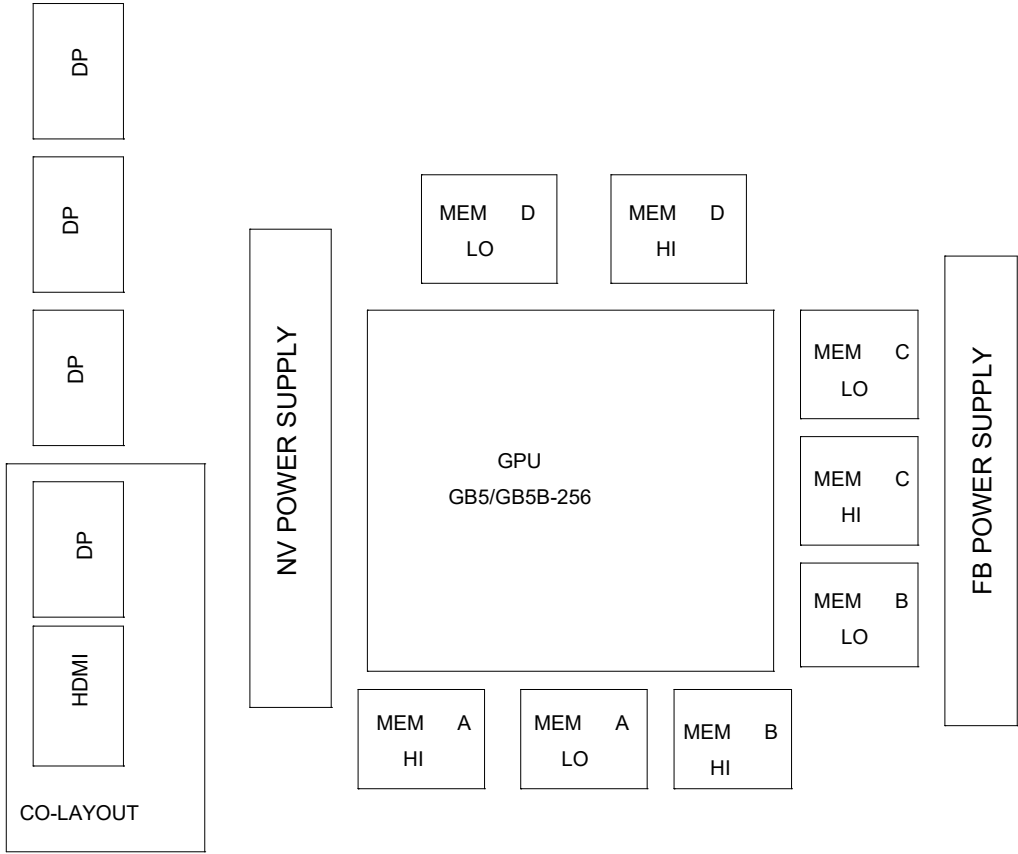
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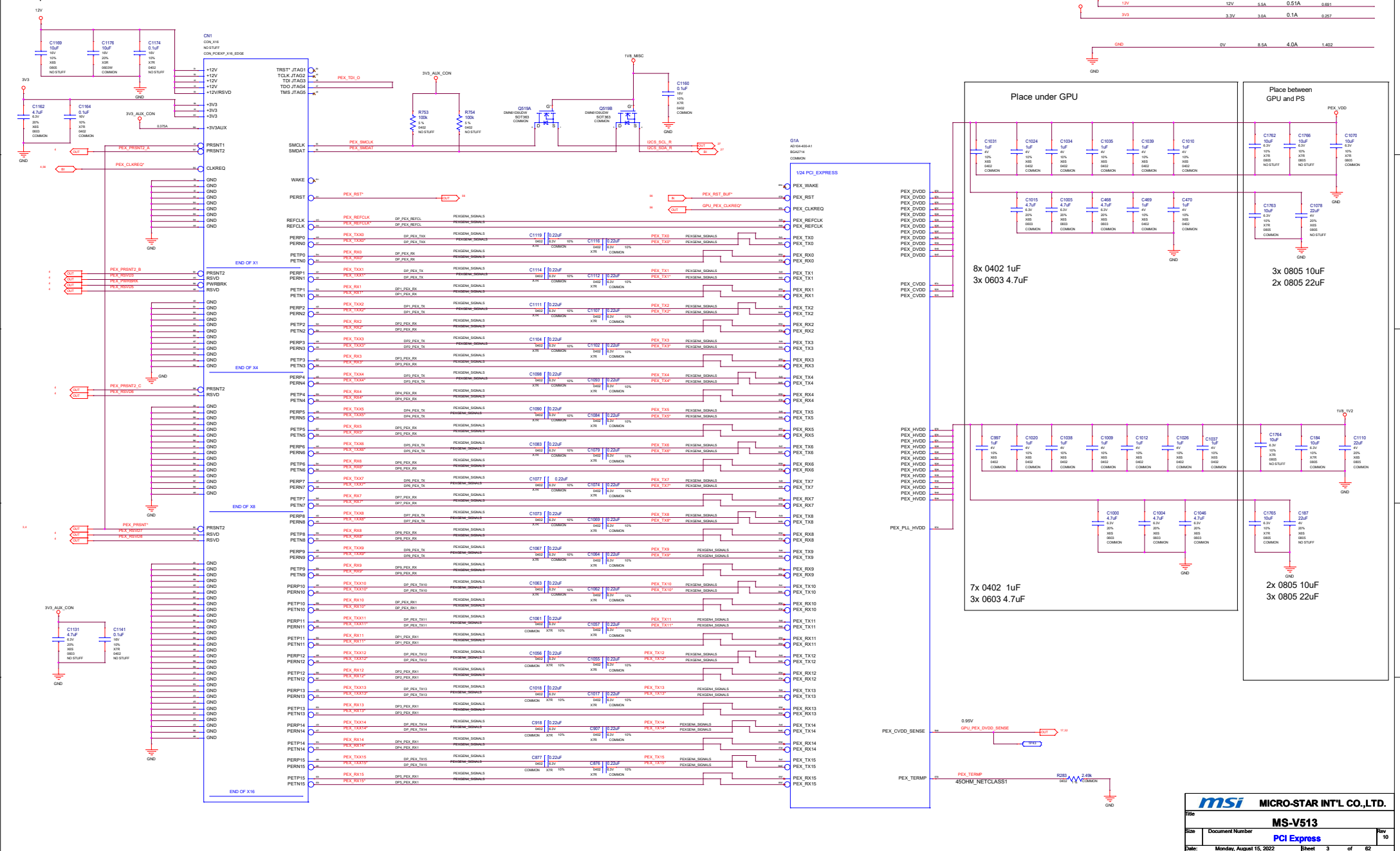
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Block Diagram



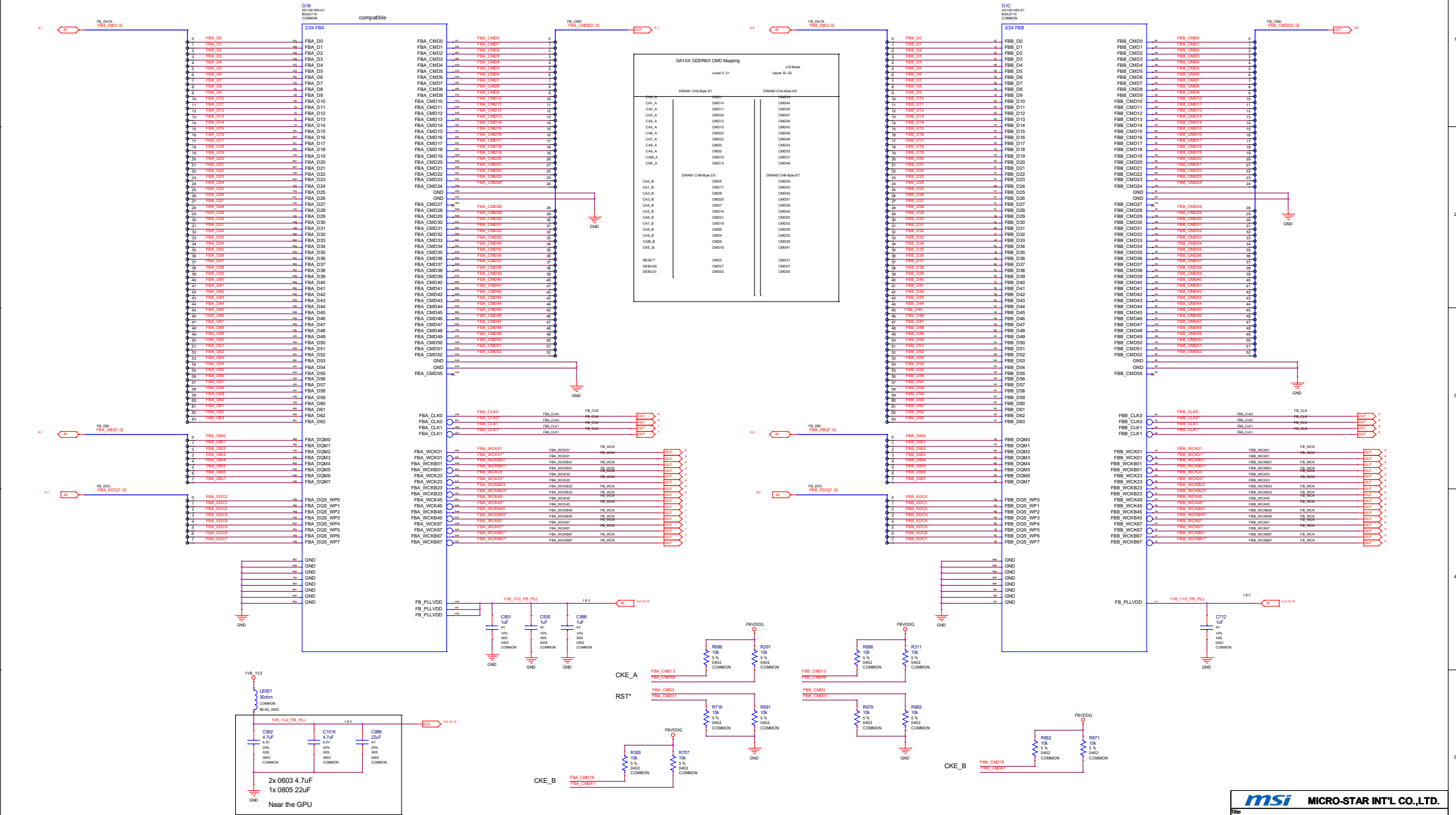
PCI Express



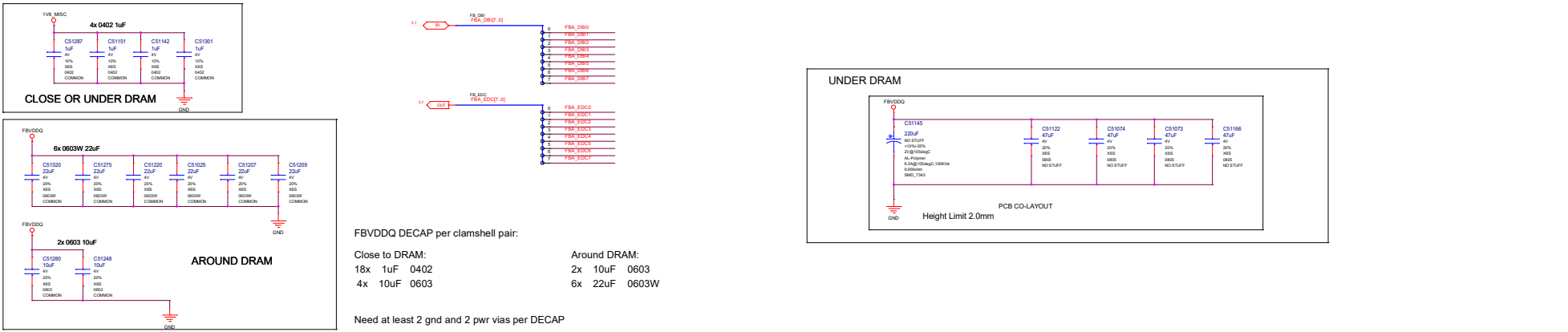
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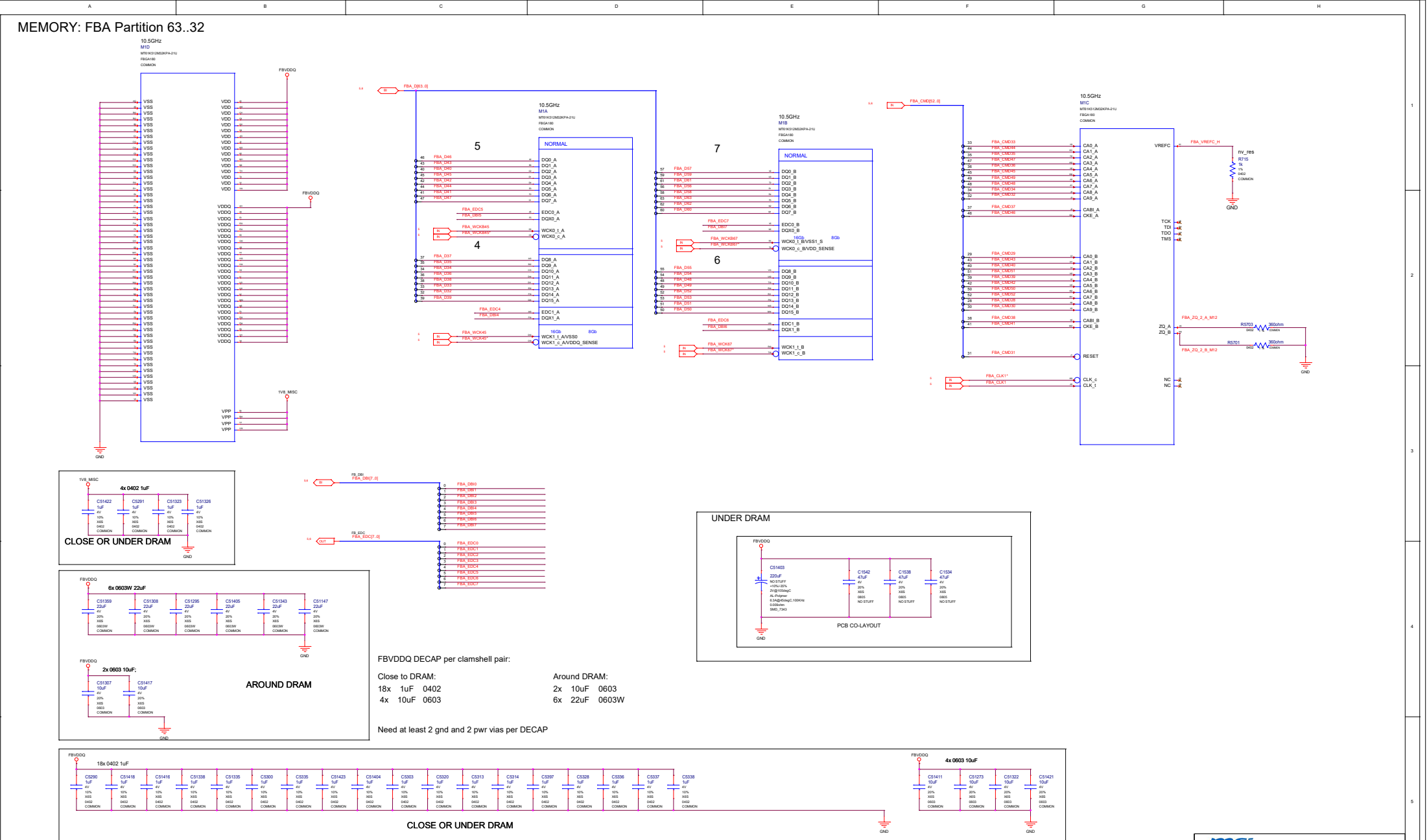
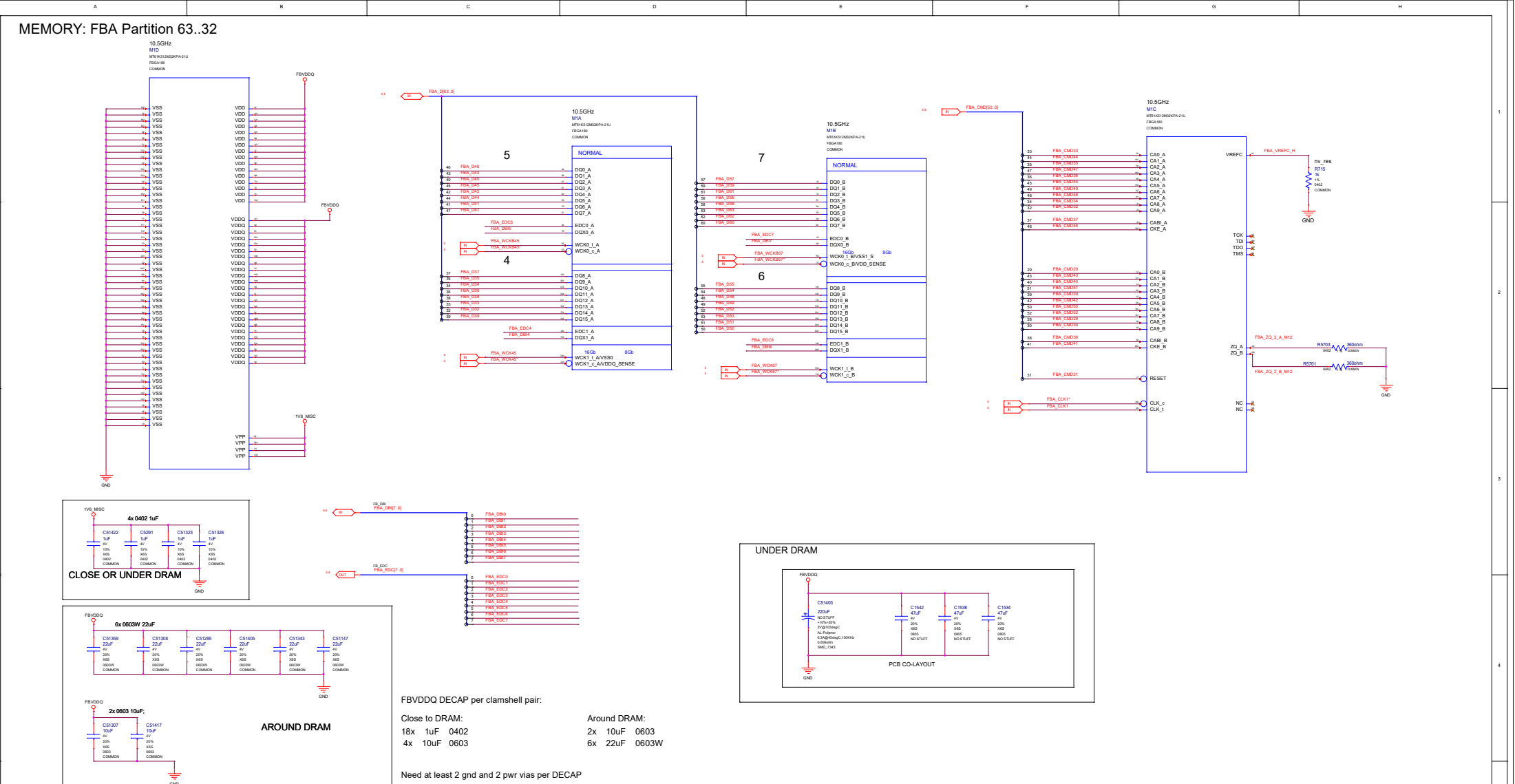
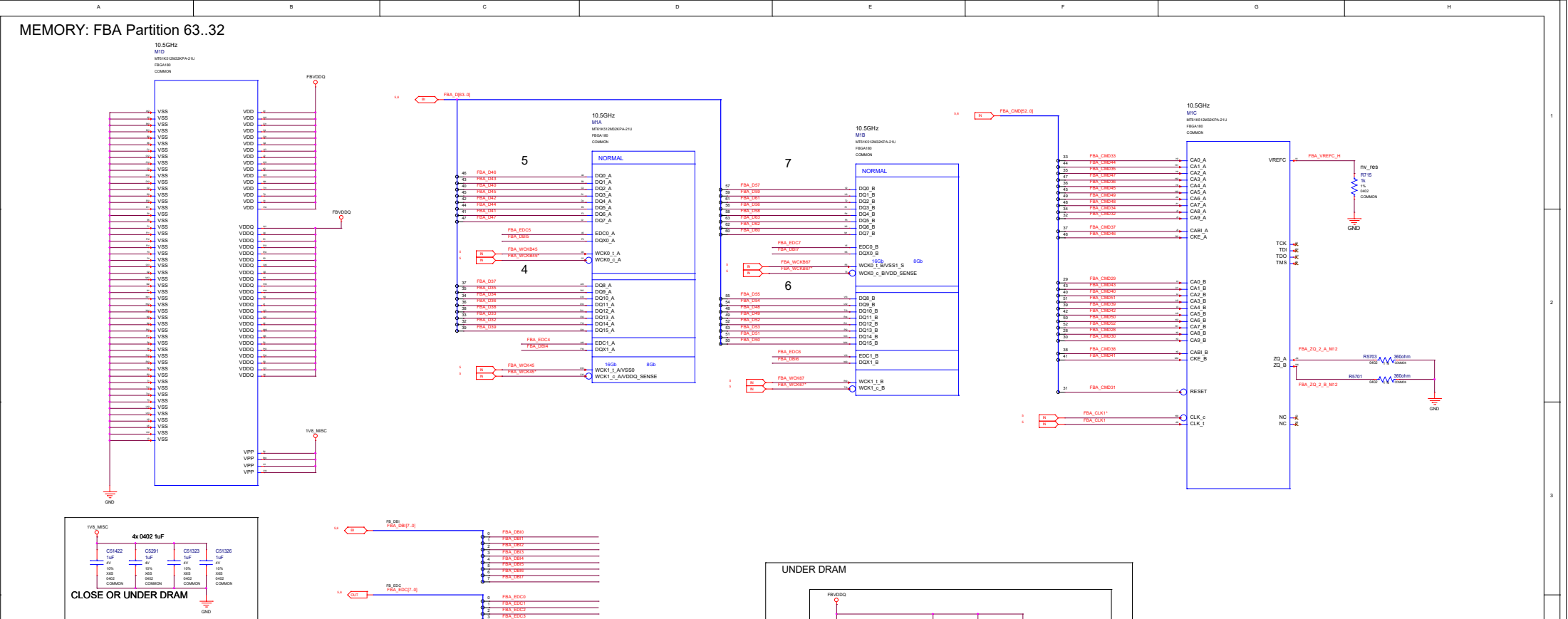
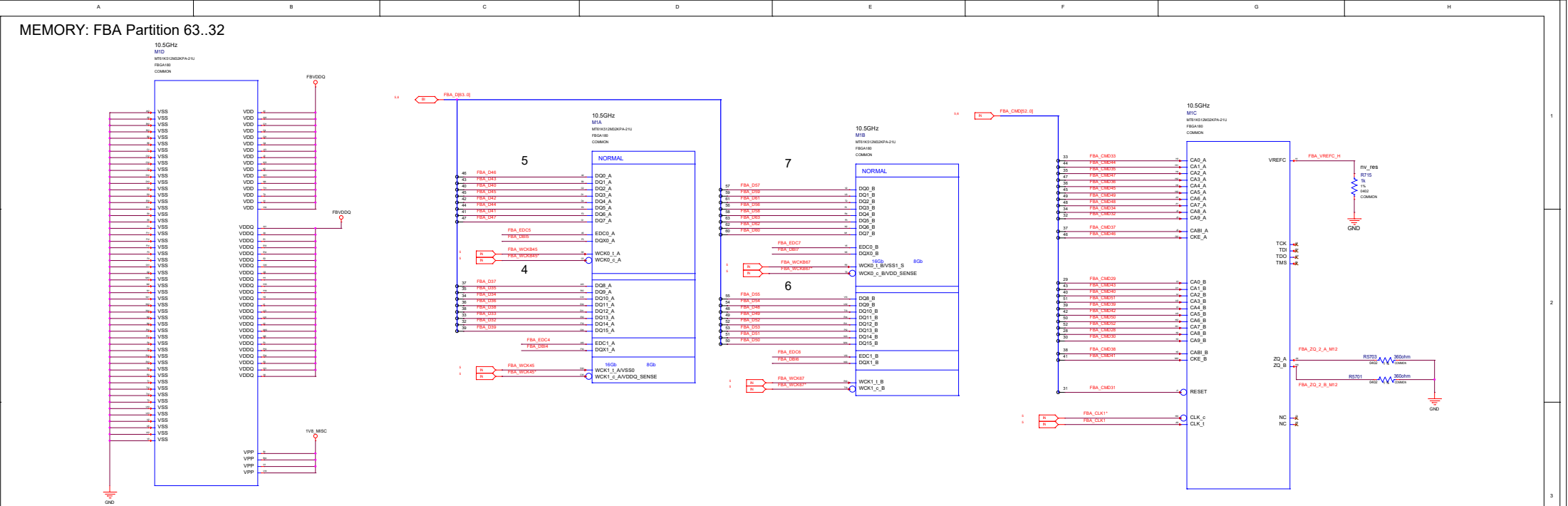
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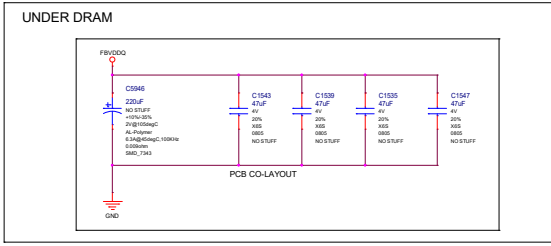
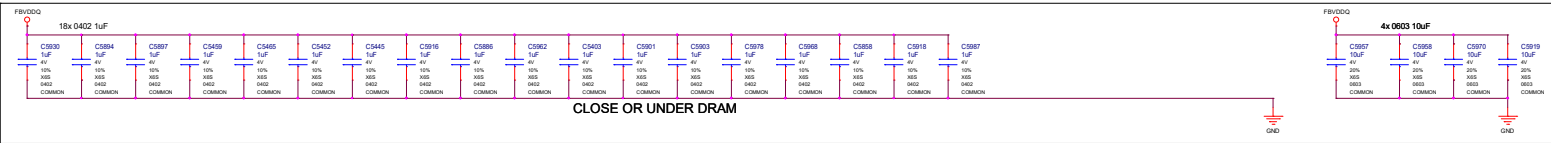
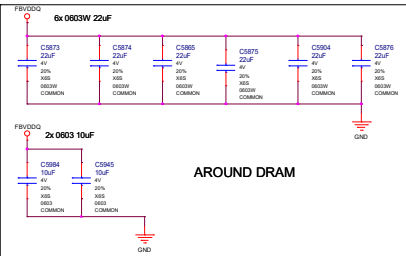
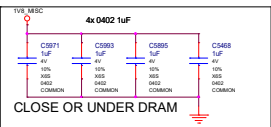
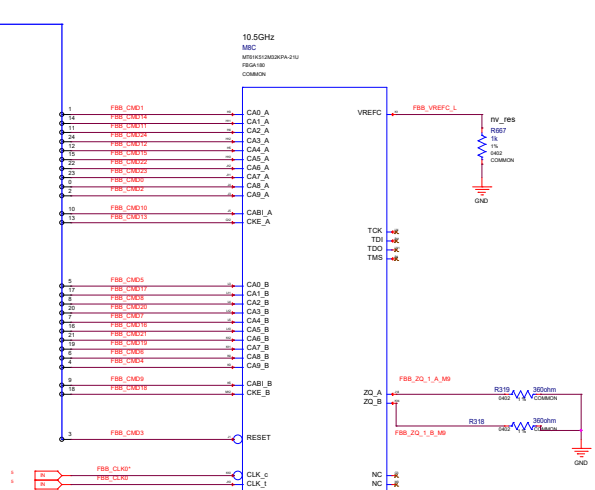
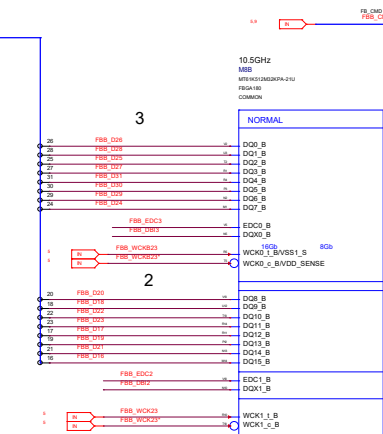
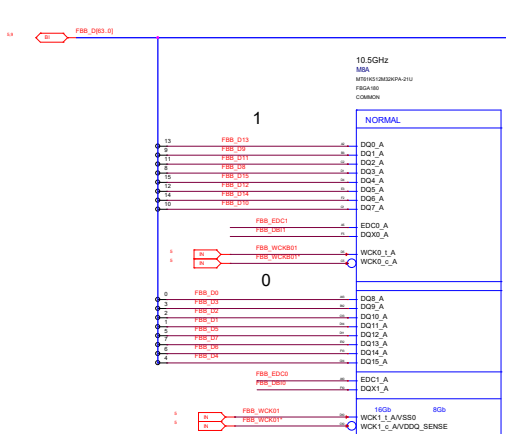
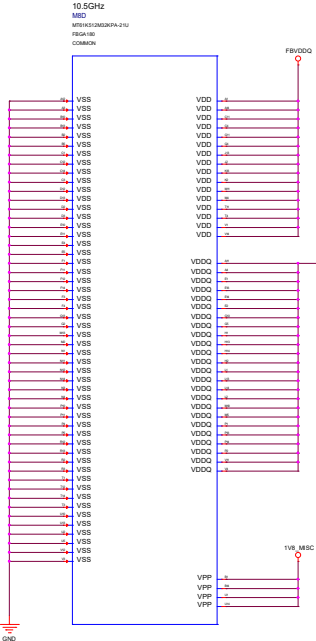
A	B	C	D	E	F	G	H
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A	B	C	D	E	F	G	H
---	---	---	---	---	---	---	---



MEMORY: FBB Partition 31..0



FBVDDQ DECAP per clamshell pair:

Close to DRAM:

18x 1uF 0402

4x 10uF 0603

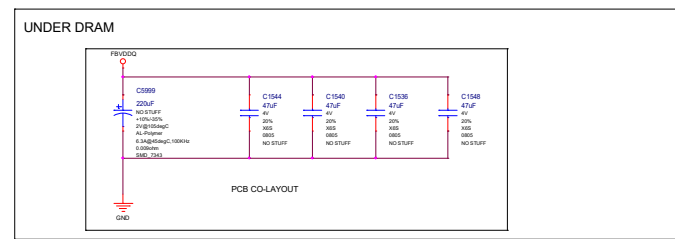
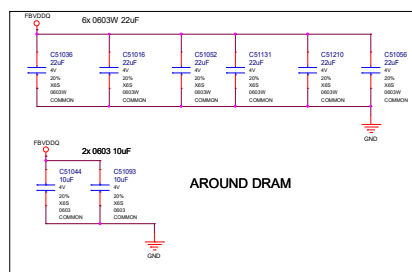
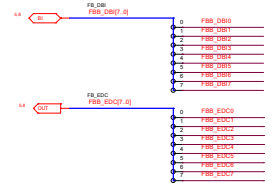
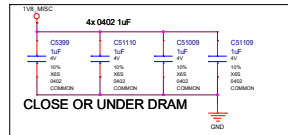
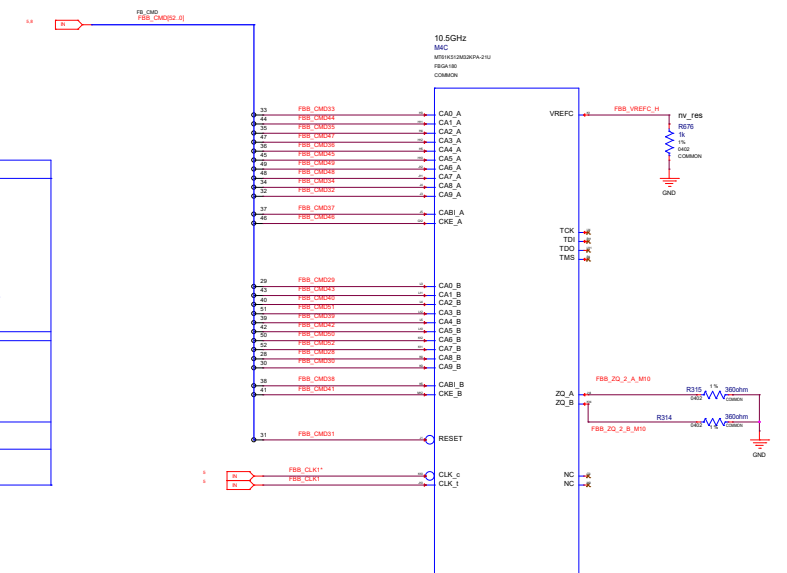
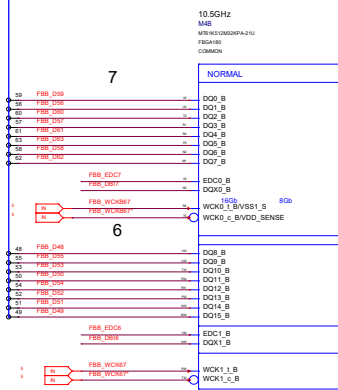
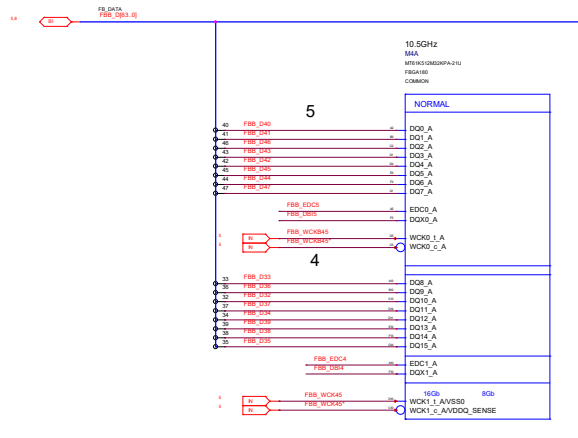
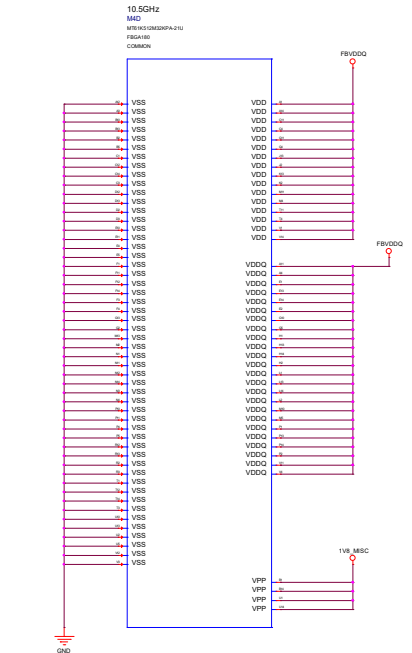
Around DRAM:

2x 10uF 0603

6x 22uF 0603W

Need at least 2 gnd and 2 pwr vias per DECAP

MEMORY: FBB Partition 63..32



FBVDDQ DECAP per clamshell pair:

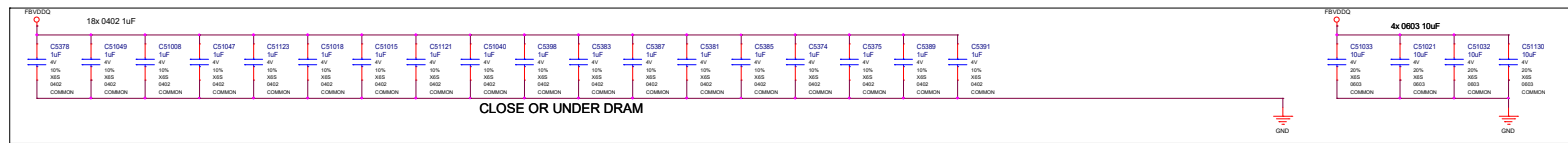
Close to DRAM:


18x	1uF	0402
4x	10uF	0603

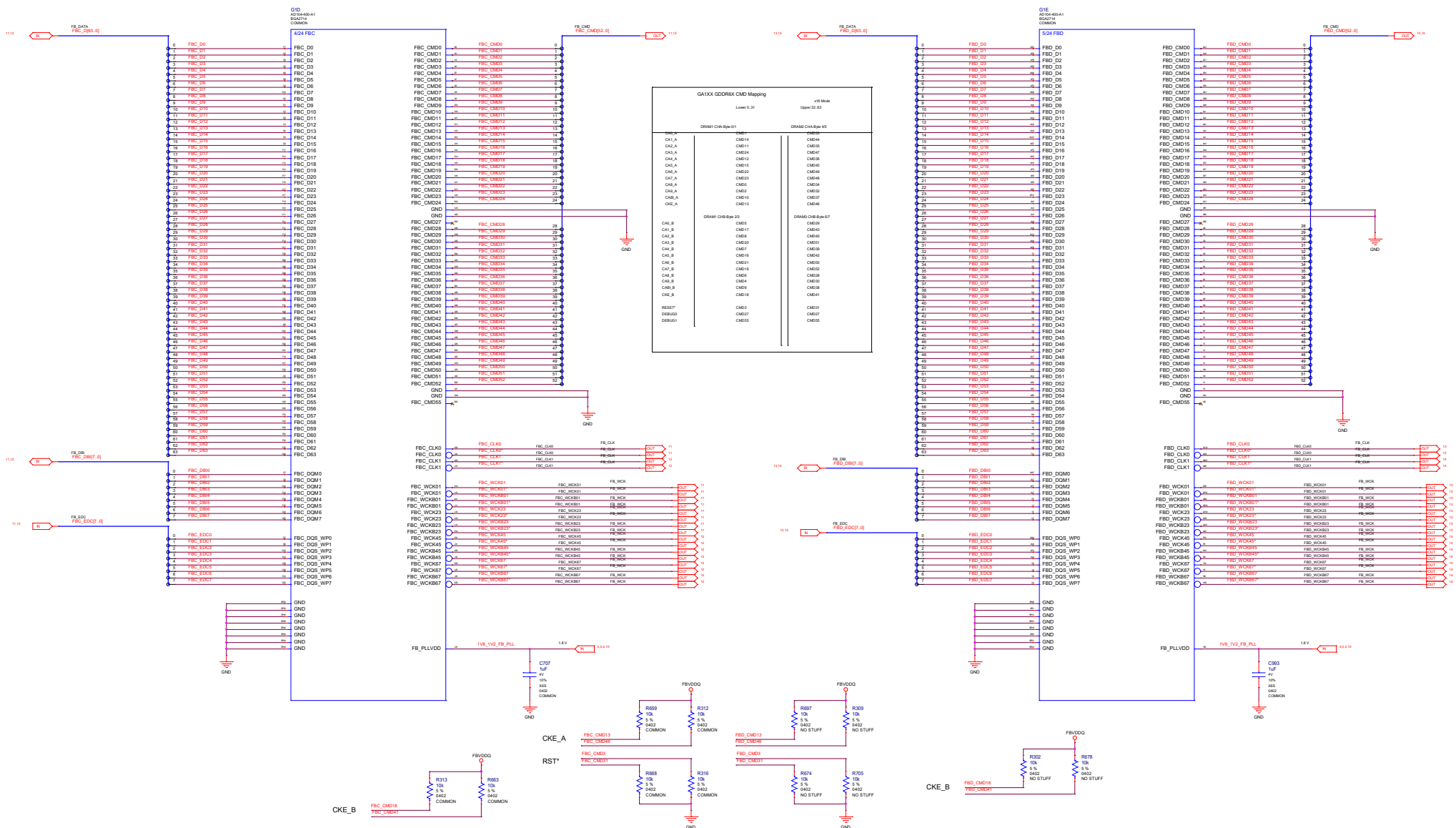
Around DRAM:

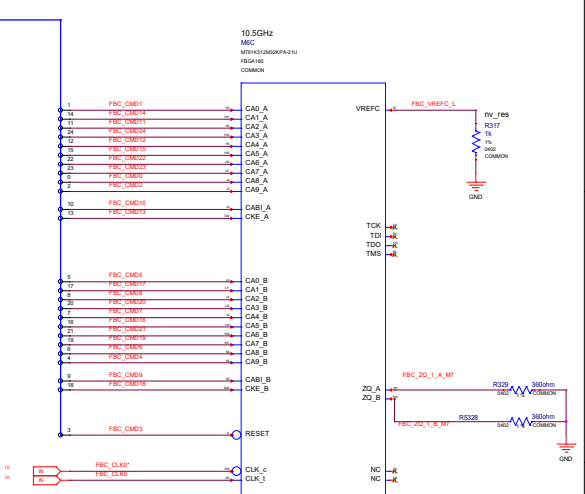
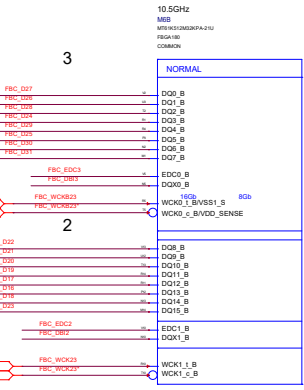
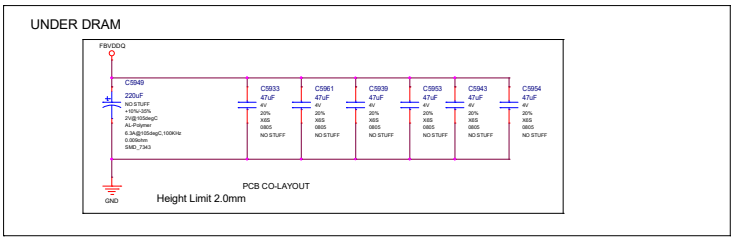
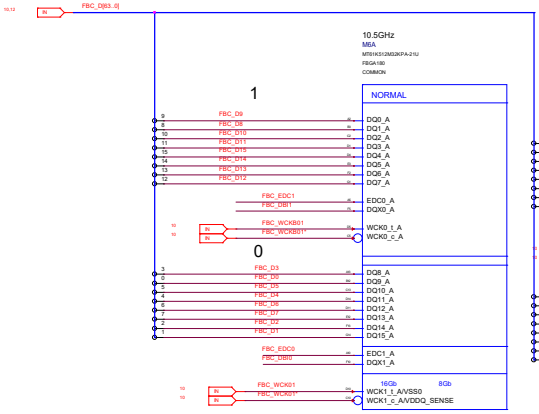
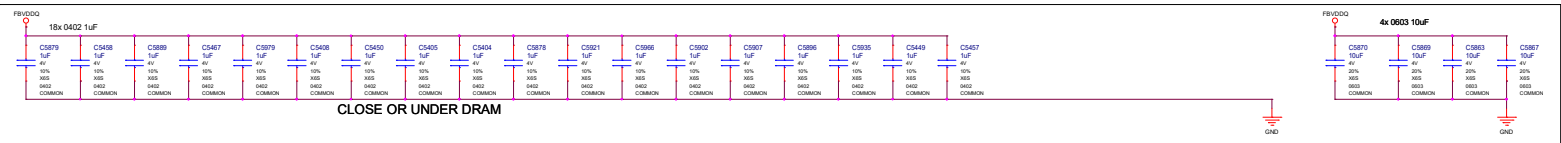
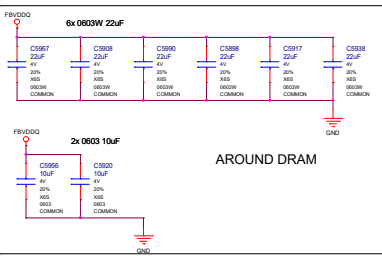
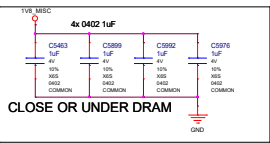
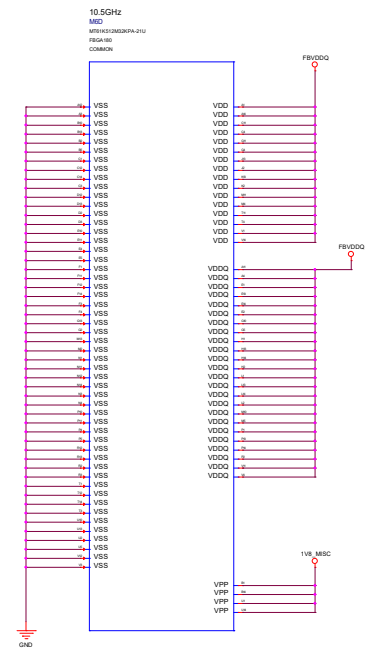
2x	10uF	0603
6x	22uF	0603W

Need at least 2 gnd and 2 pwr vias per DECAP



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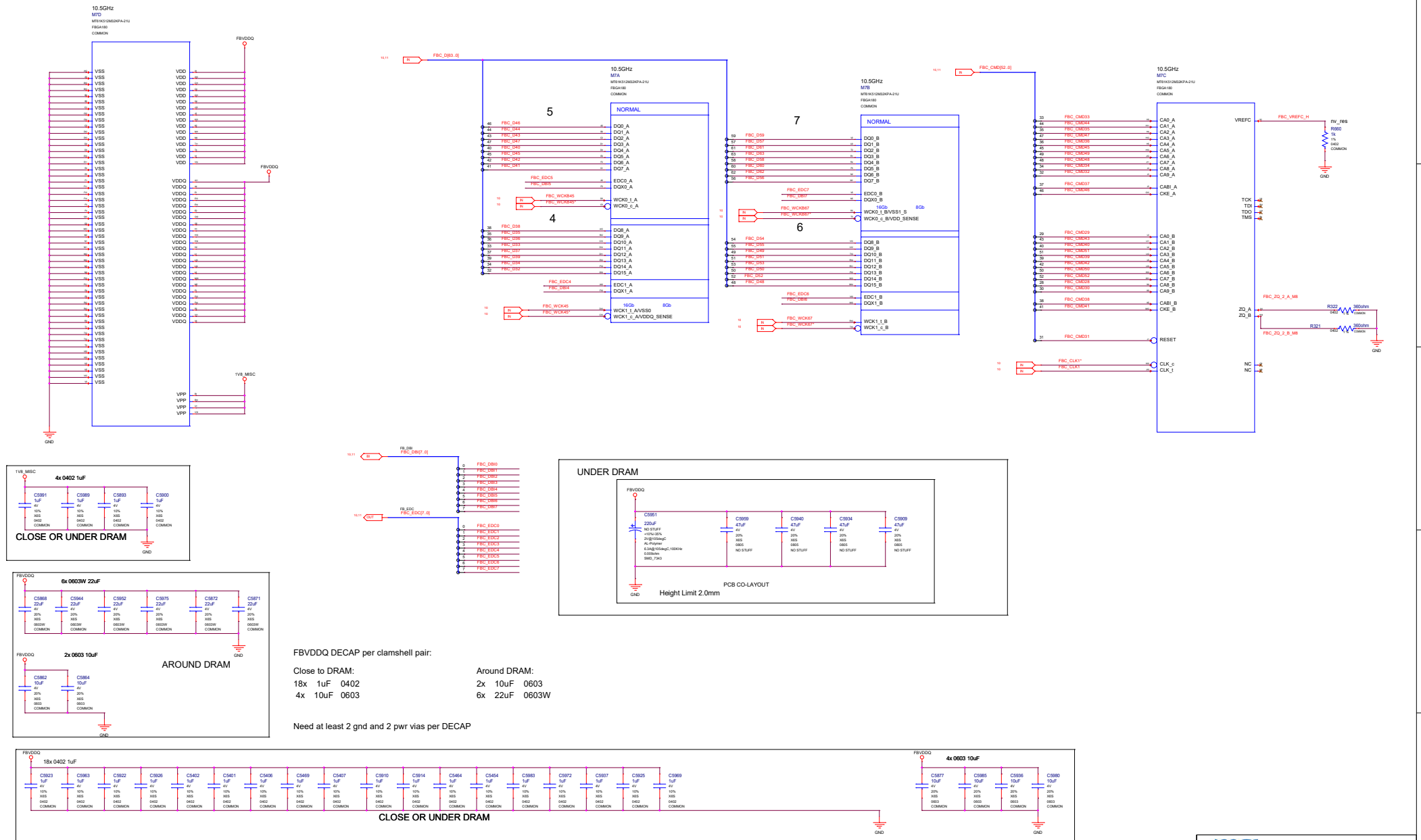


FBVDDQ DECAP per clamshell pair:

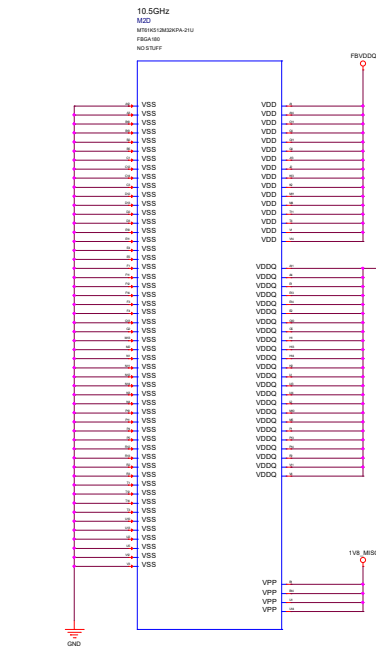
Close to DRAM:	Around DRAM:
18x 1uF 0402	2x 10uF 0603
4x 10uF 0603	6x 22uF 0603W

Need at least 2 gnd and 2 pwr vias per DECAP

MEMORY: FBC Partition 63..32



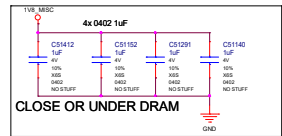
MEMORY: FBD Partition 31..0



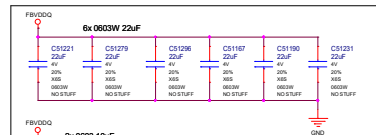
FBVDDQ

FBVDDQ

TVB_MISC



CLOSE OR UNDER DRAM



AROUND DRAM

FBVDDQ

2x 0603 10uF

C51232

C51129

FBVDDQ DECAP per clamshell pair:

Close to DRAM:

18x 1uF 0402

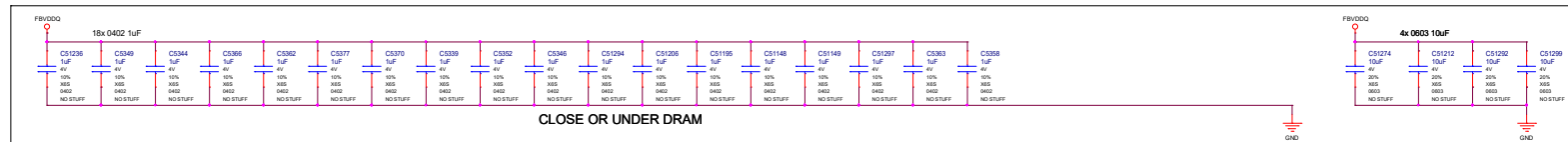
4x 10uF 0603

Around DRAM:

2x 10uF 0603

6x 22uF 0603W

Need at least 2 gnd and 2 pwr vias per DECAP



CLOSE OR UNDER DRAM

FBVDDQ

4x 0603 10uF

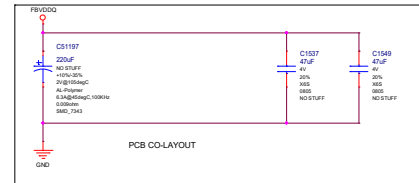
C51374

C51312

C51282

C51298

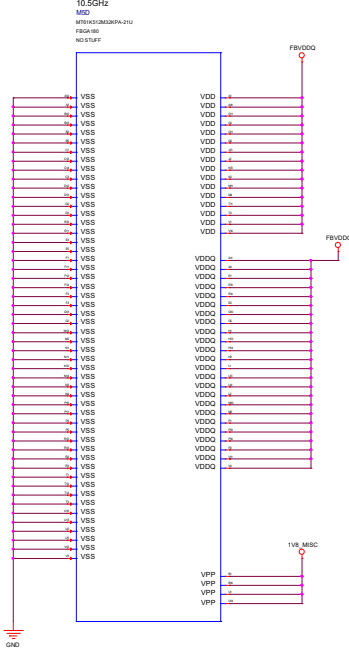
UNDER DRAM



PCB CO-LAYOUT

msi MICRO-STAR INT'L CO.,LTD.			
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MEMORY: FBD Partition 63..32



FBD_D03_0

FBD_D03_0

FBD_D03_0

FBD_D03_0

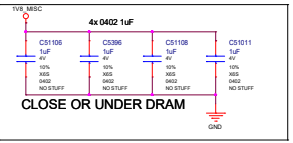
FBD_D03_0

FBD_D03_0

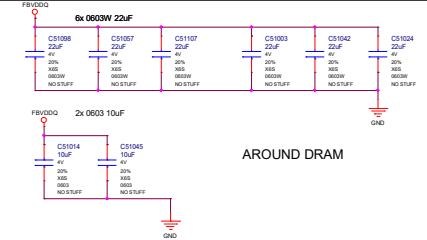
FBD_D03_0

FBD_D03_0

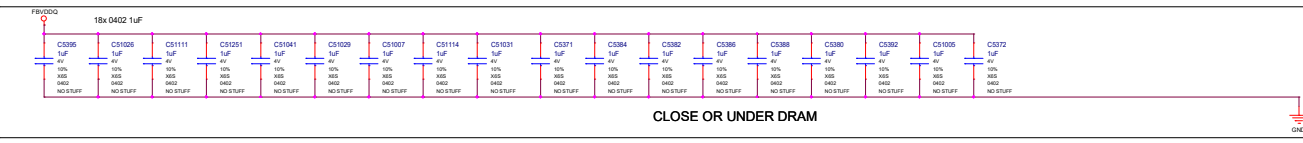
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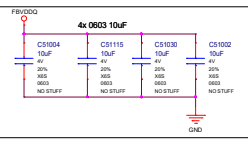
CLOSE OR UNDER DRAM



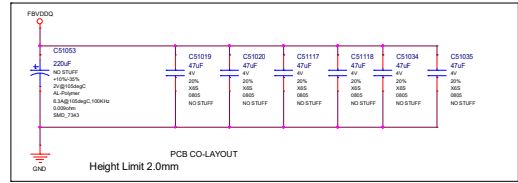
AROUND DRAM



CLOSE OR UNDER DRAM



UNDER DRAM



PCB CO-LAYOUT
Height Limit 2.0mm

FBDVDDQ DECAP per clamshell pair:

Close to DRAM:

18x 1uF 0402

4x 10uF 0603

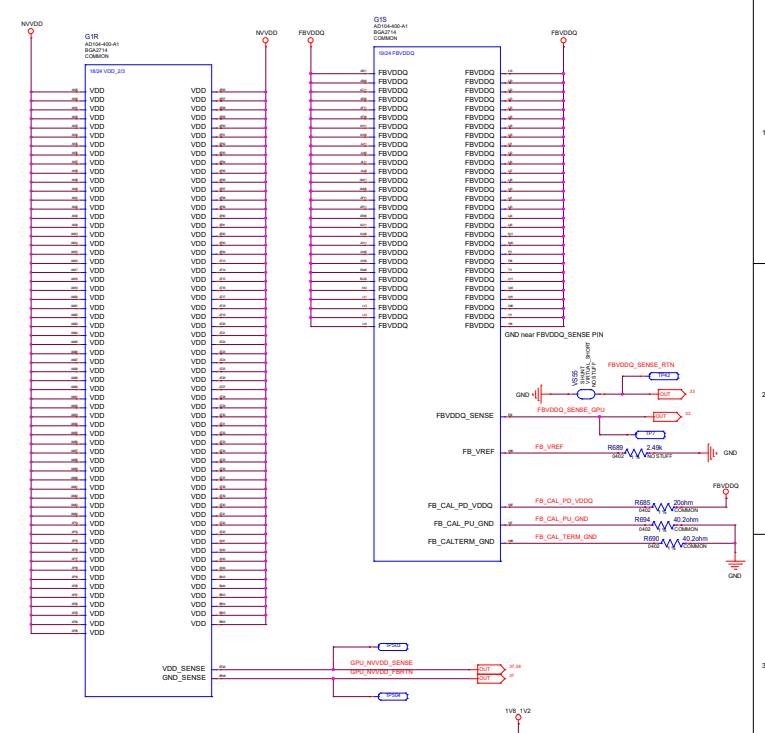
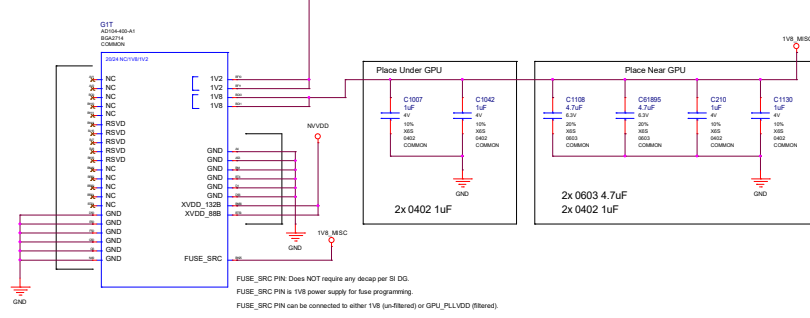
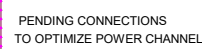
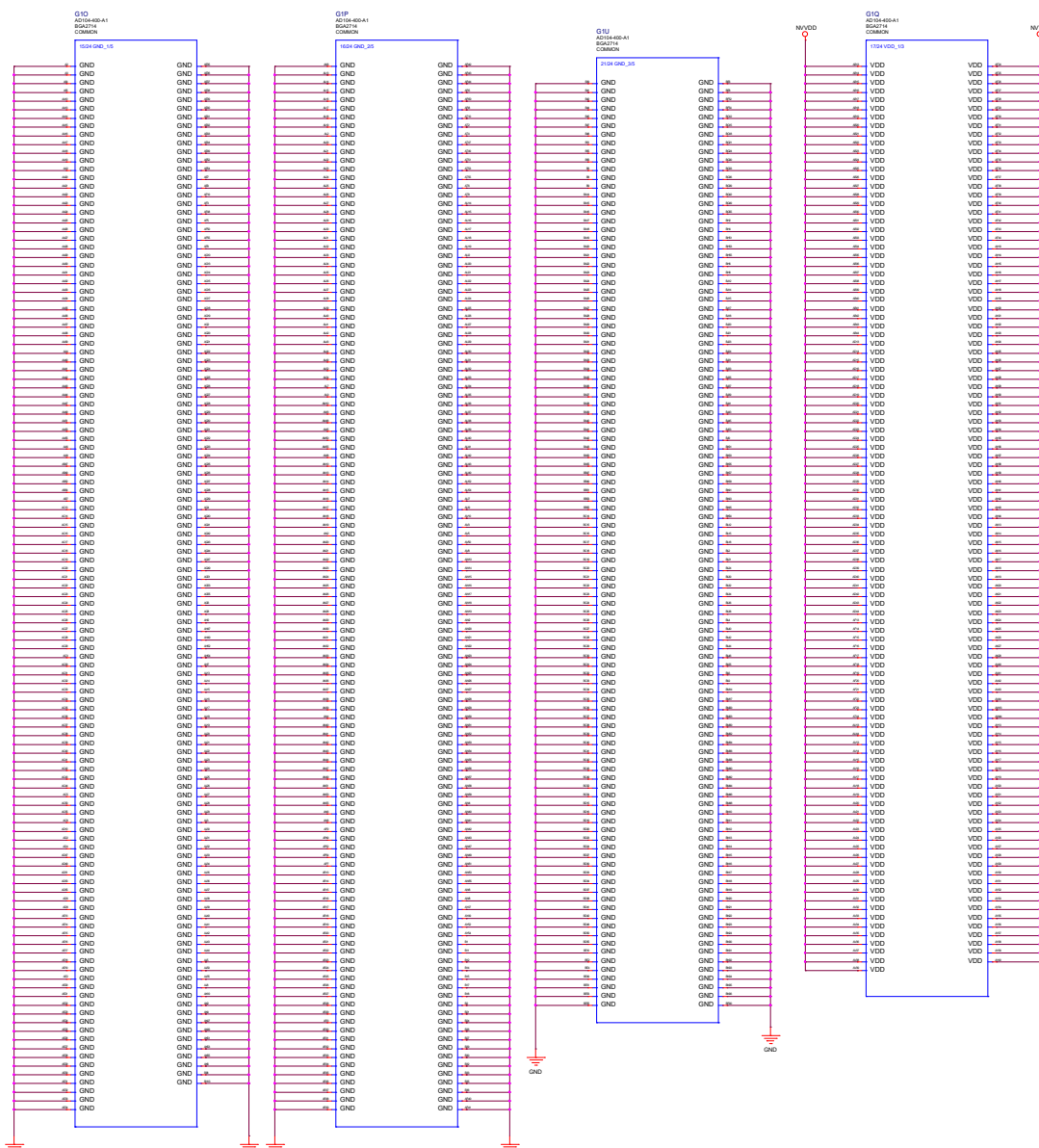
Around DRAM:


2x 10uF 0603

6x 22uF 0603W

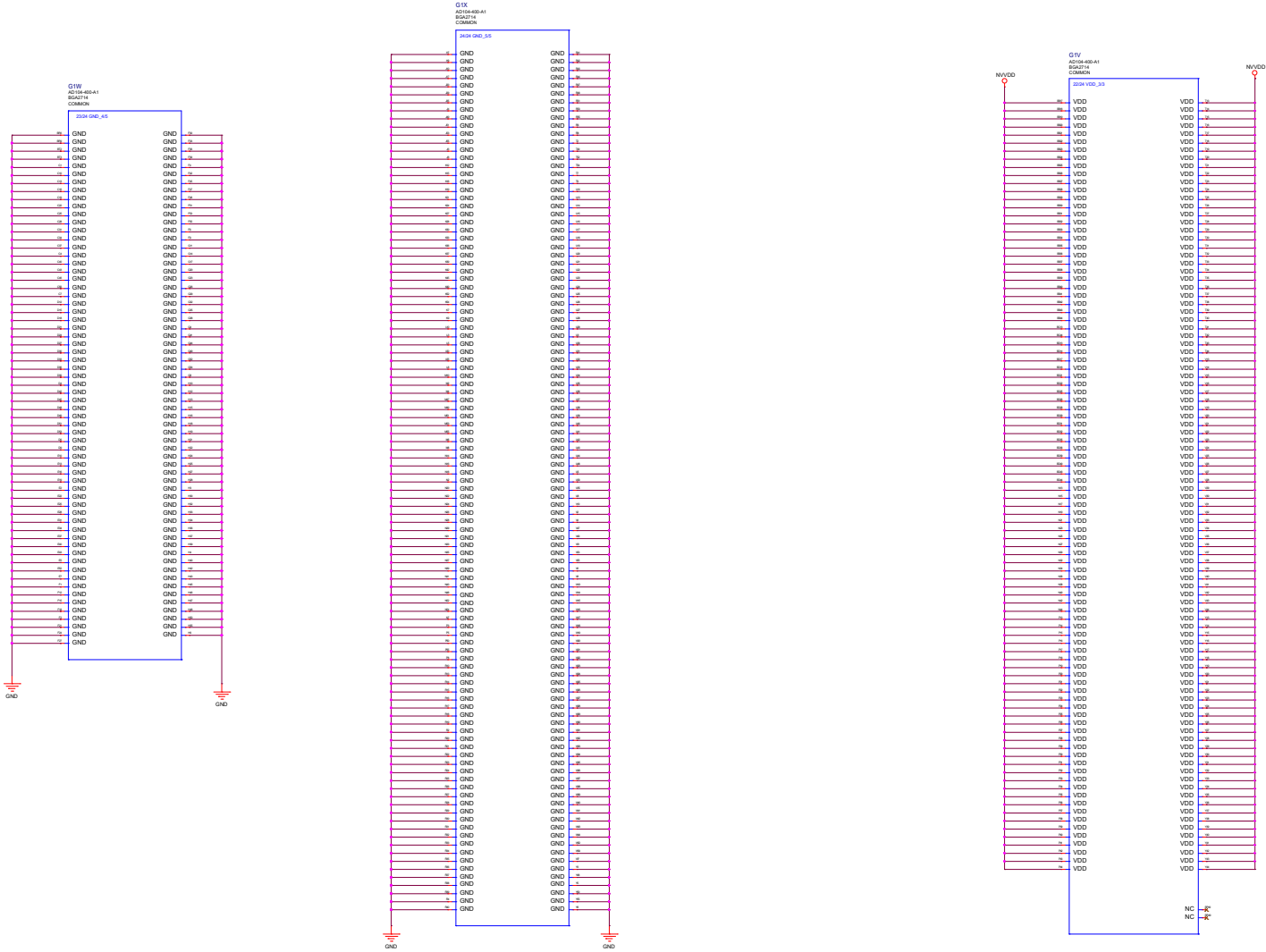
Need at least 2 gnd and 2 pwr vias per DECAP

GPU PWR and GND

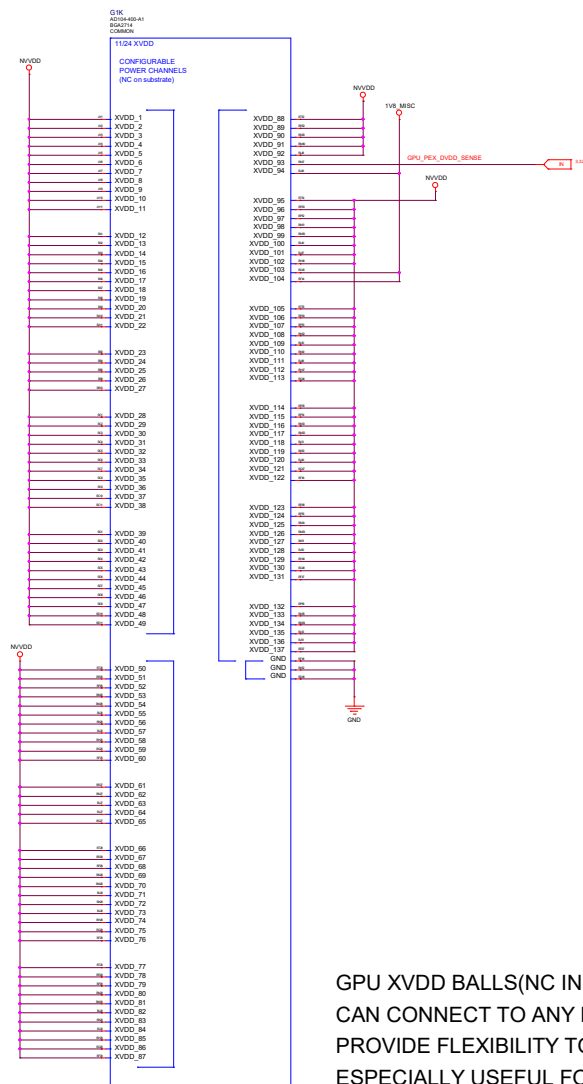


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GPU PWR and GND 2

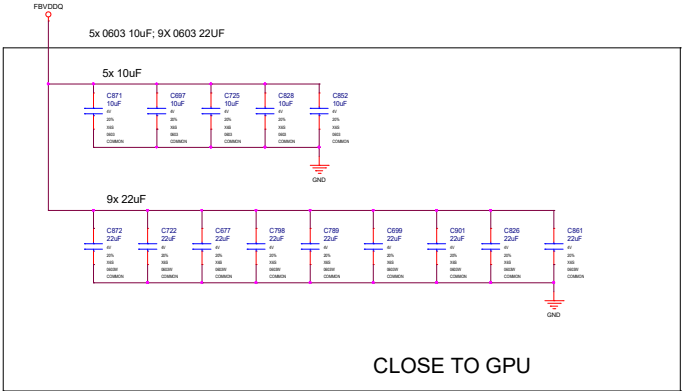
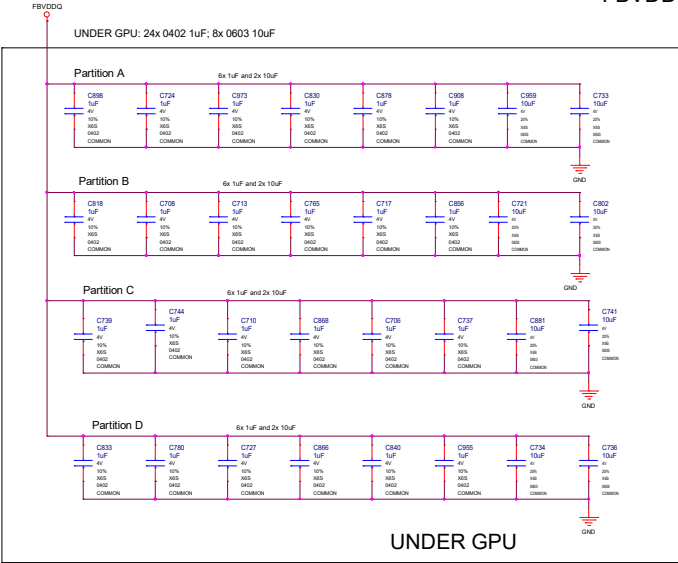


XVDD



GPU DECOUPLING FBVDDQ

FBVDDQ




GPU DECOUPLING NVDD



UNDER GPU

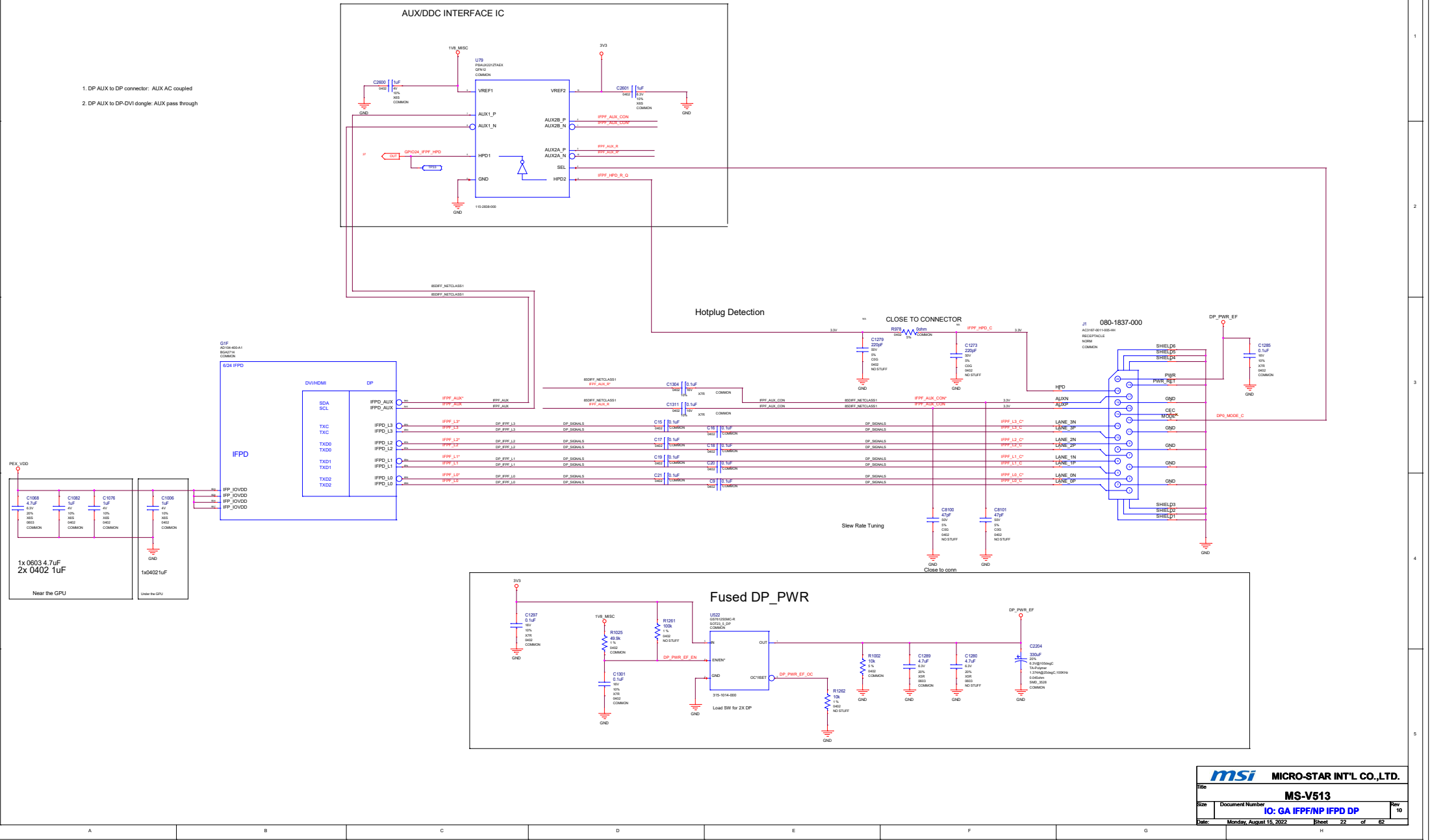
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UNDER GPU

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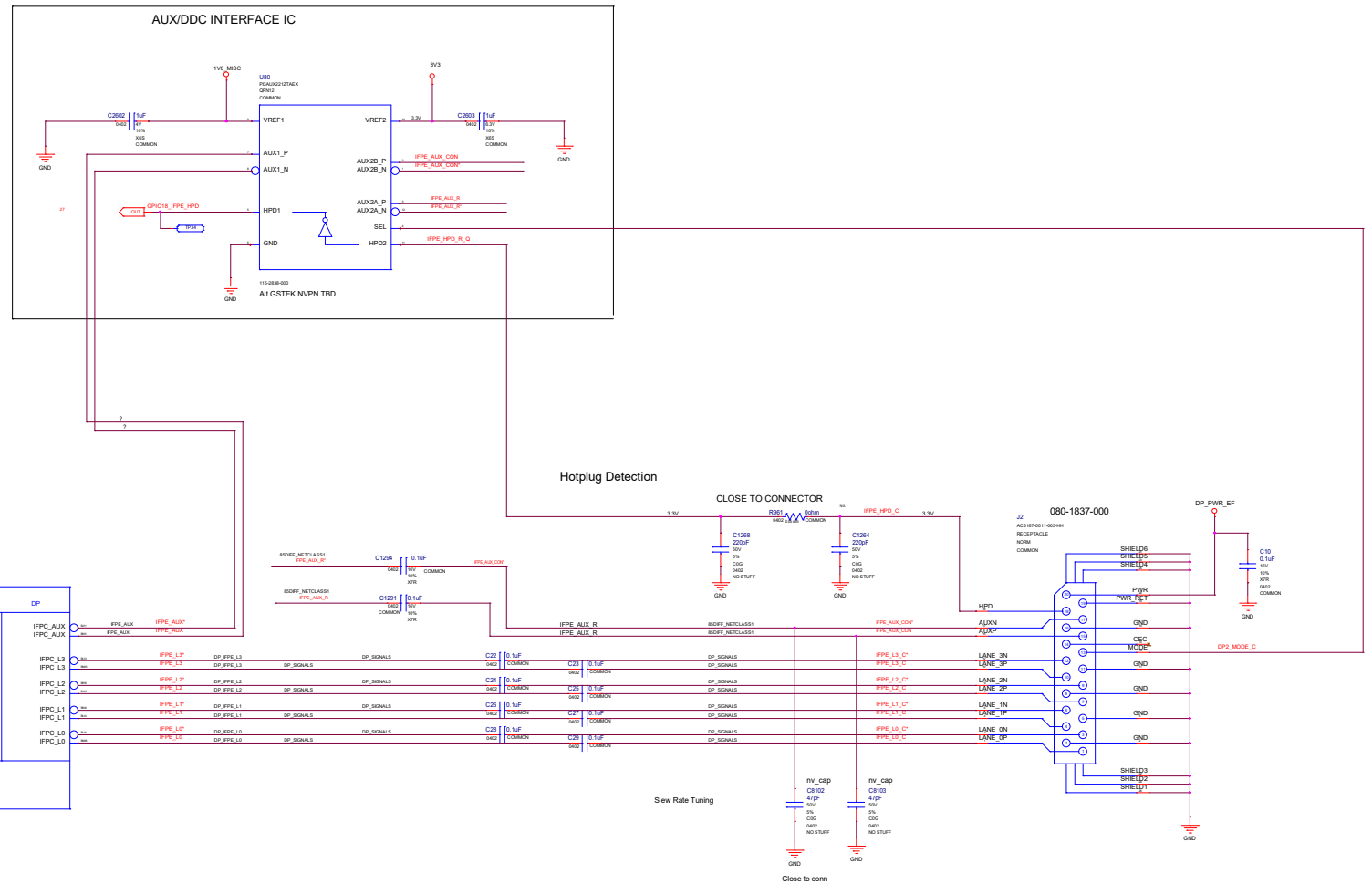
GA IFPF/NP IFPD DP

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through

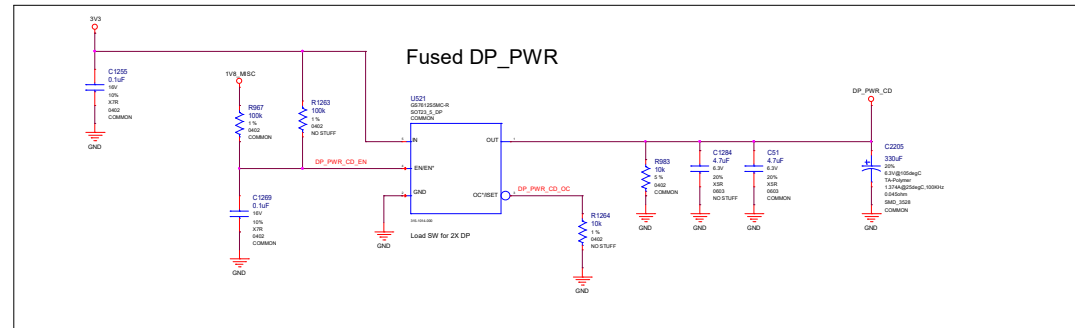
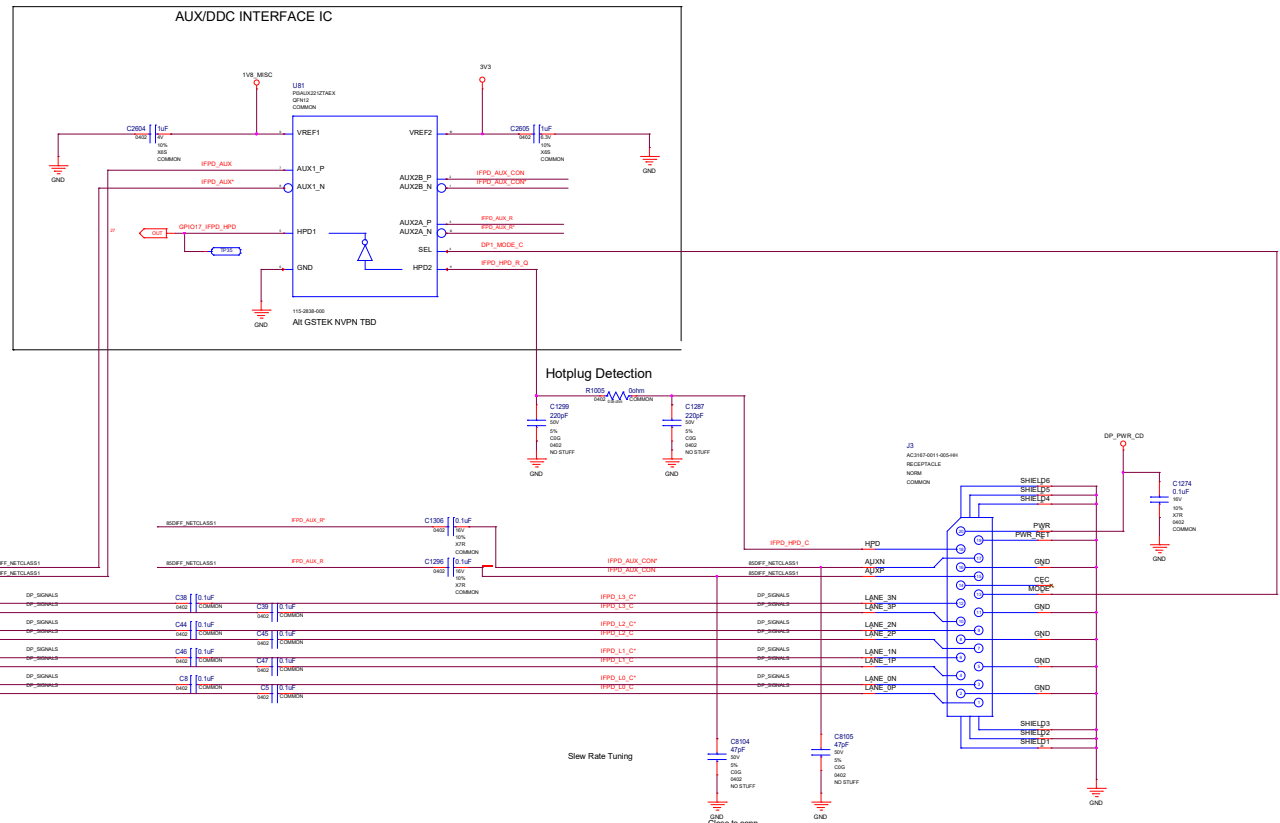


GA IFPE/NP IFPC DP

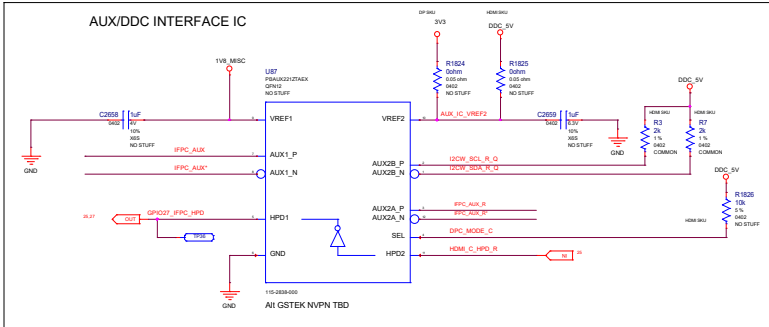
1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



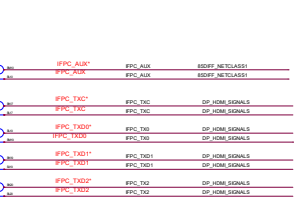
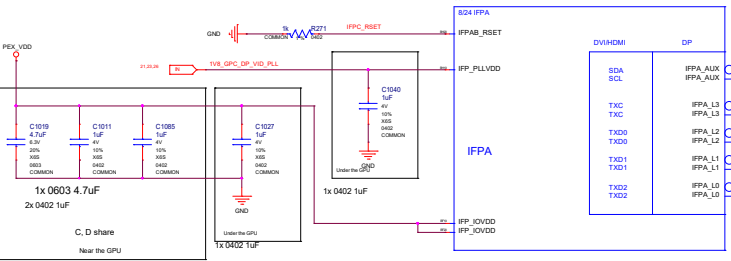
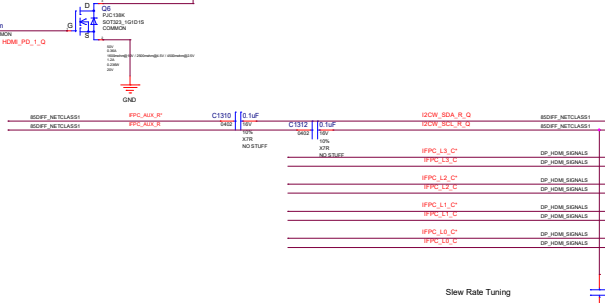
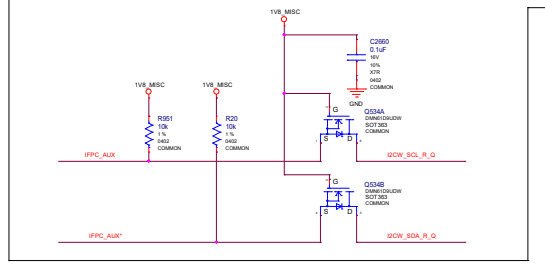
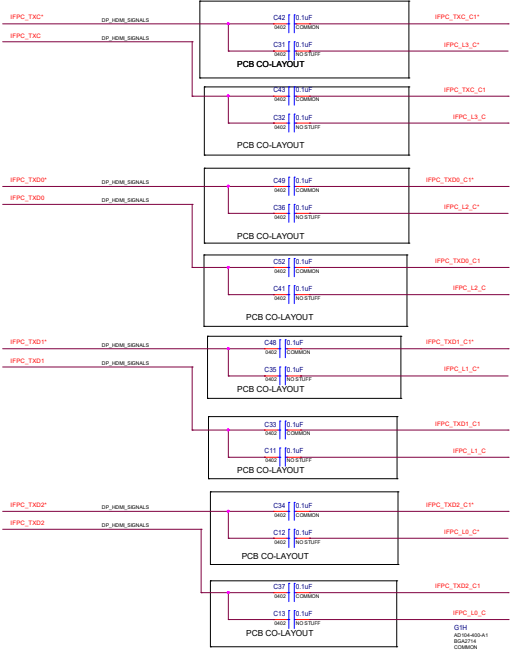
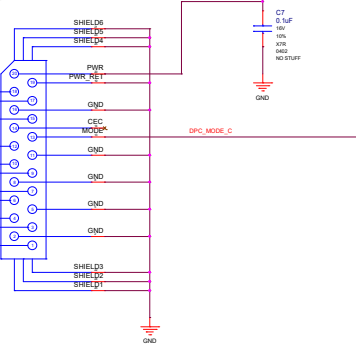
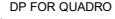
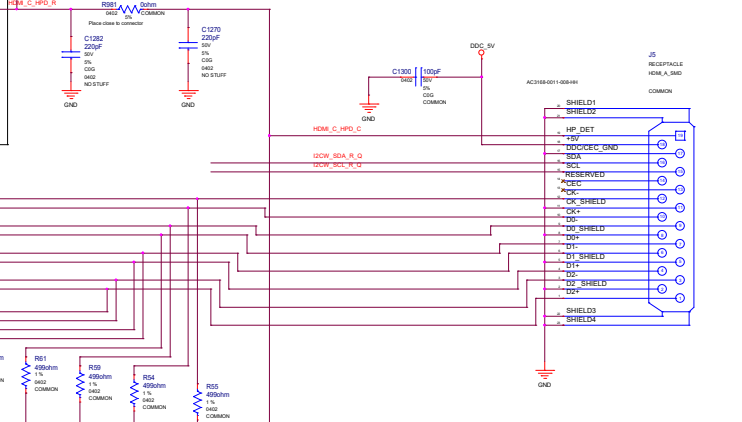
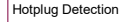
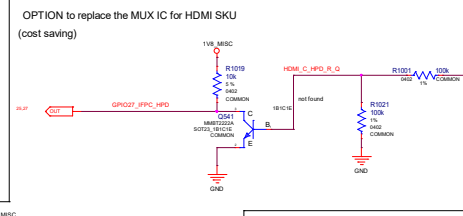
1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



GA IFPC/NP IFPA HDMI/DP co-layout



1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



 MICRO-STAR INT'L CO.,LTD.	
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MISC2: ROM, XTAL, Straps

GROUP0				
STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG MICRON 16Gb G6X 24Gbps (161-0480-900)
L	L	H	00001	RAMCFG MICRON 16Gb G6X 21Gbps (161-0479-900)

GROUP1						
ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0].FS_OVERT	1:ENABLE 0:DISABLE		
L	M	L	1001	FAN0/1=33%33%	FS_OVERT ENABLE	<-DEFAULT

GROUP2						
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

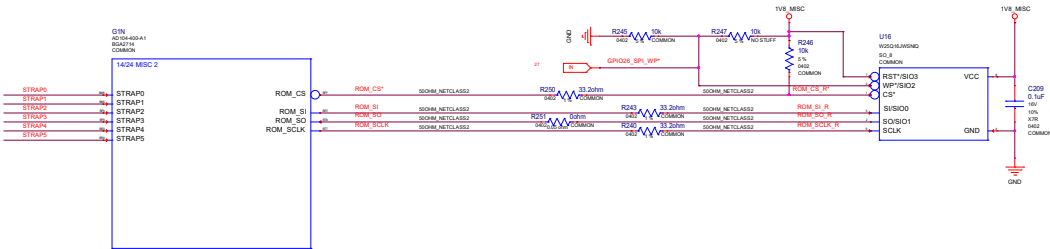
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

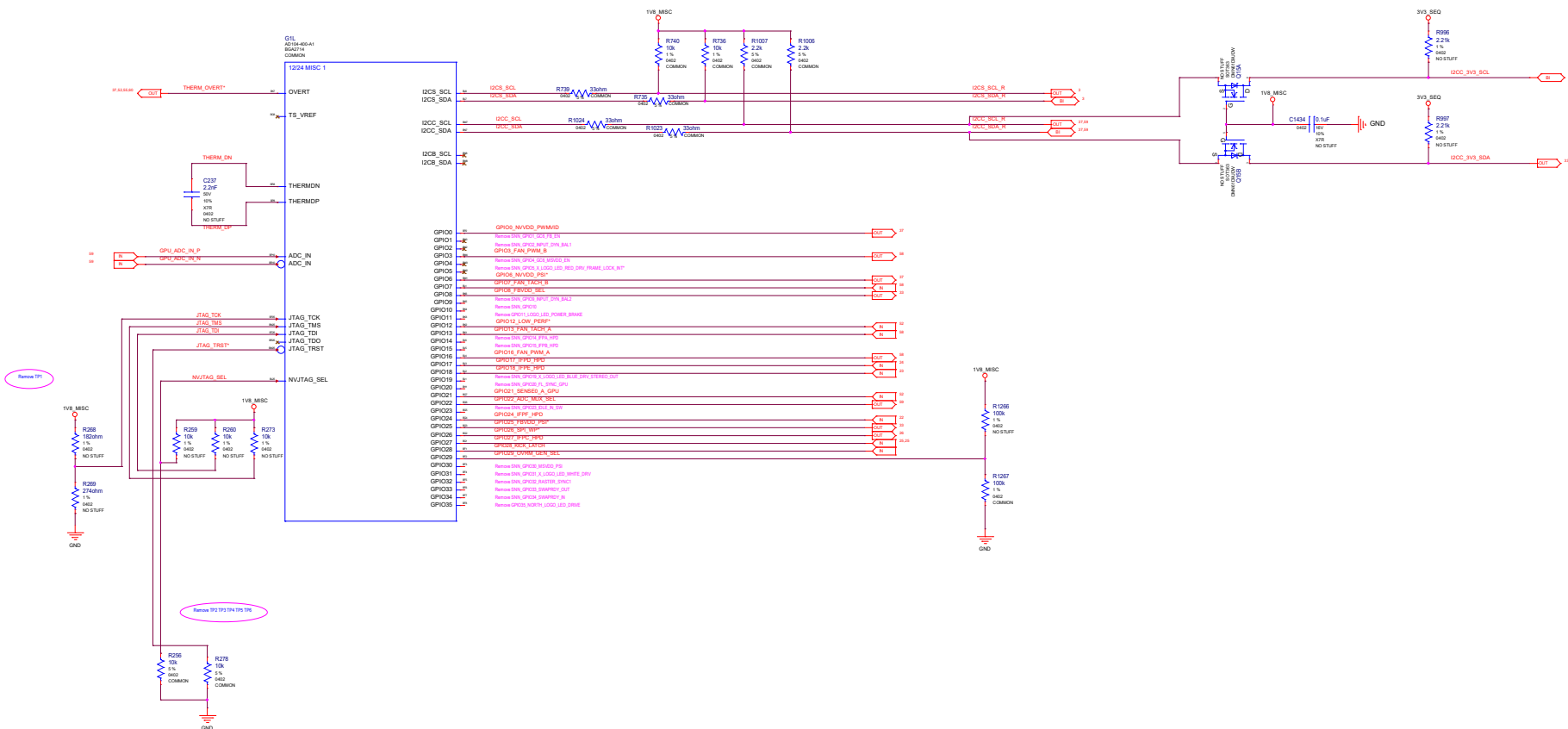
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

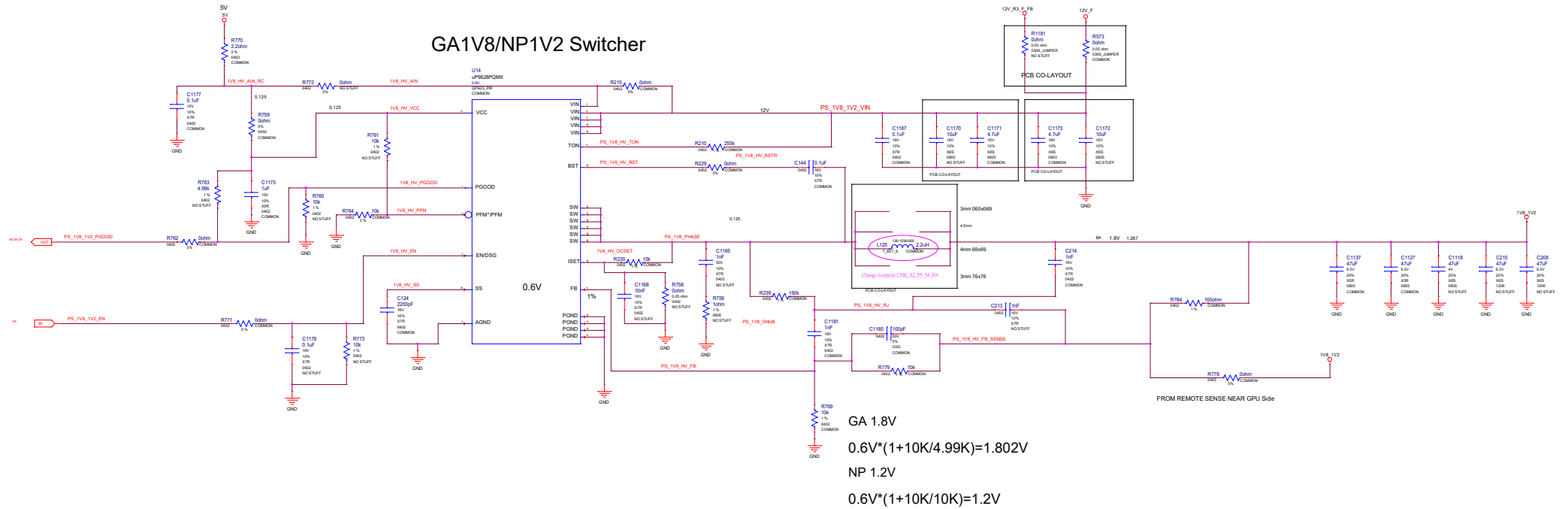


MISC1: JTAG, GPIO, ADC, I2C, OVERT

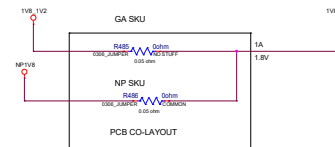
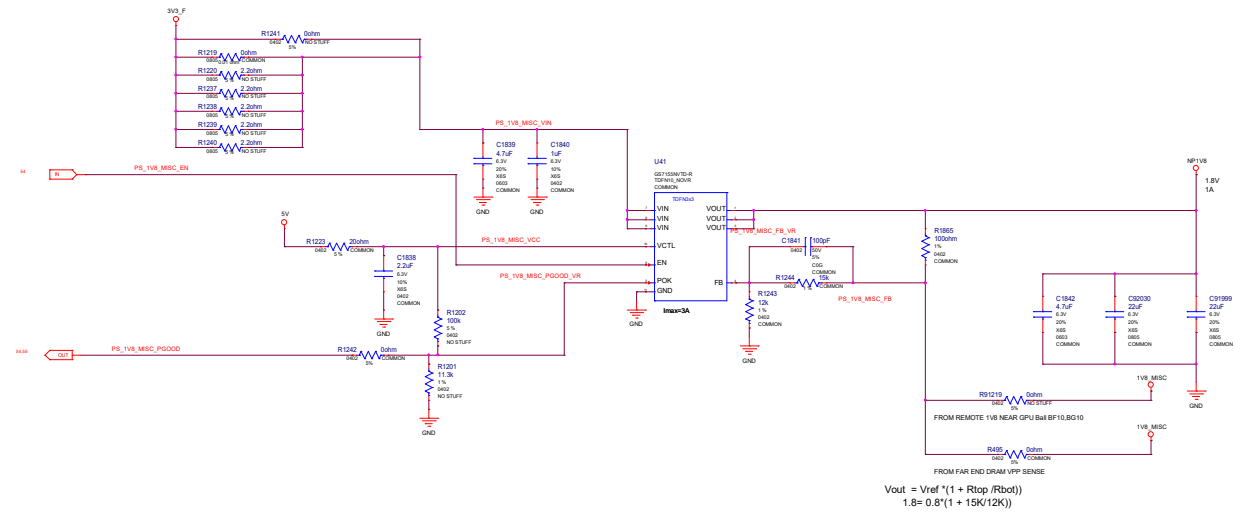


DELETED ID LED CKT; NOT SUPPORTED ON MEITNER

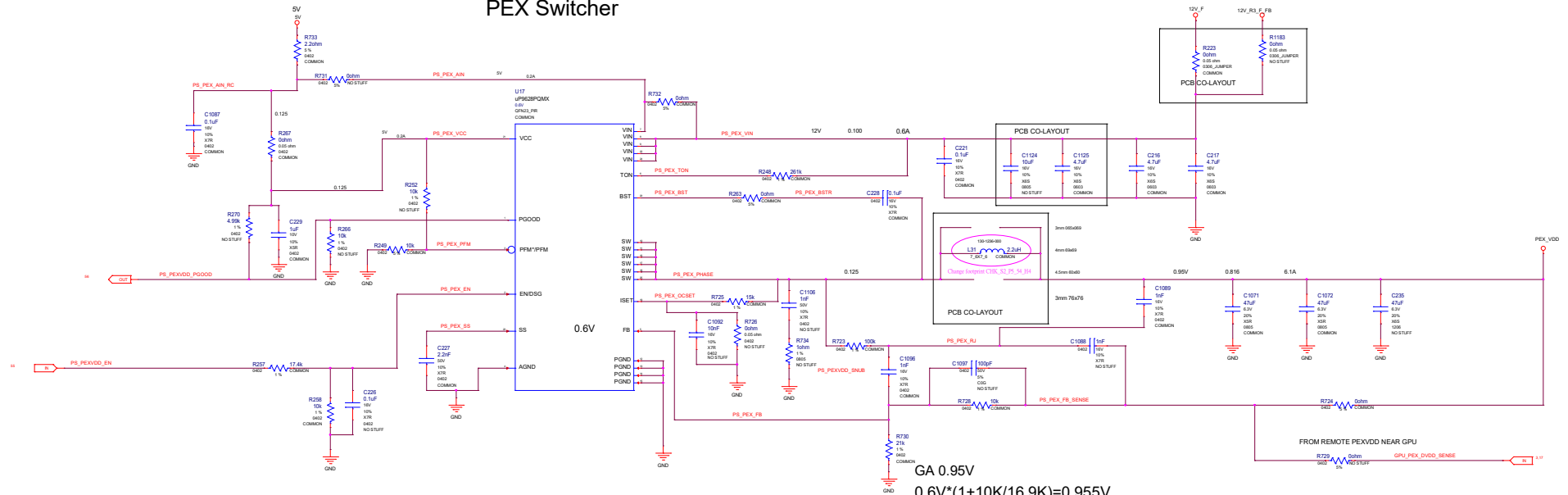
GA1V8/NP1V2 Switcher



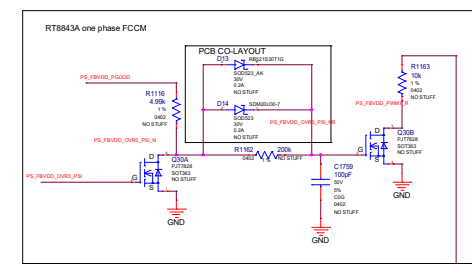
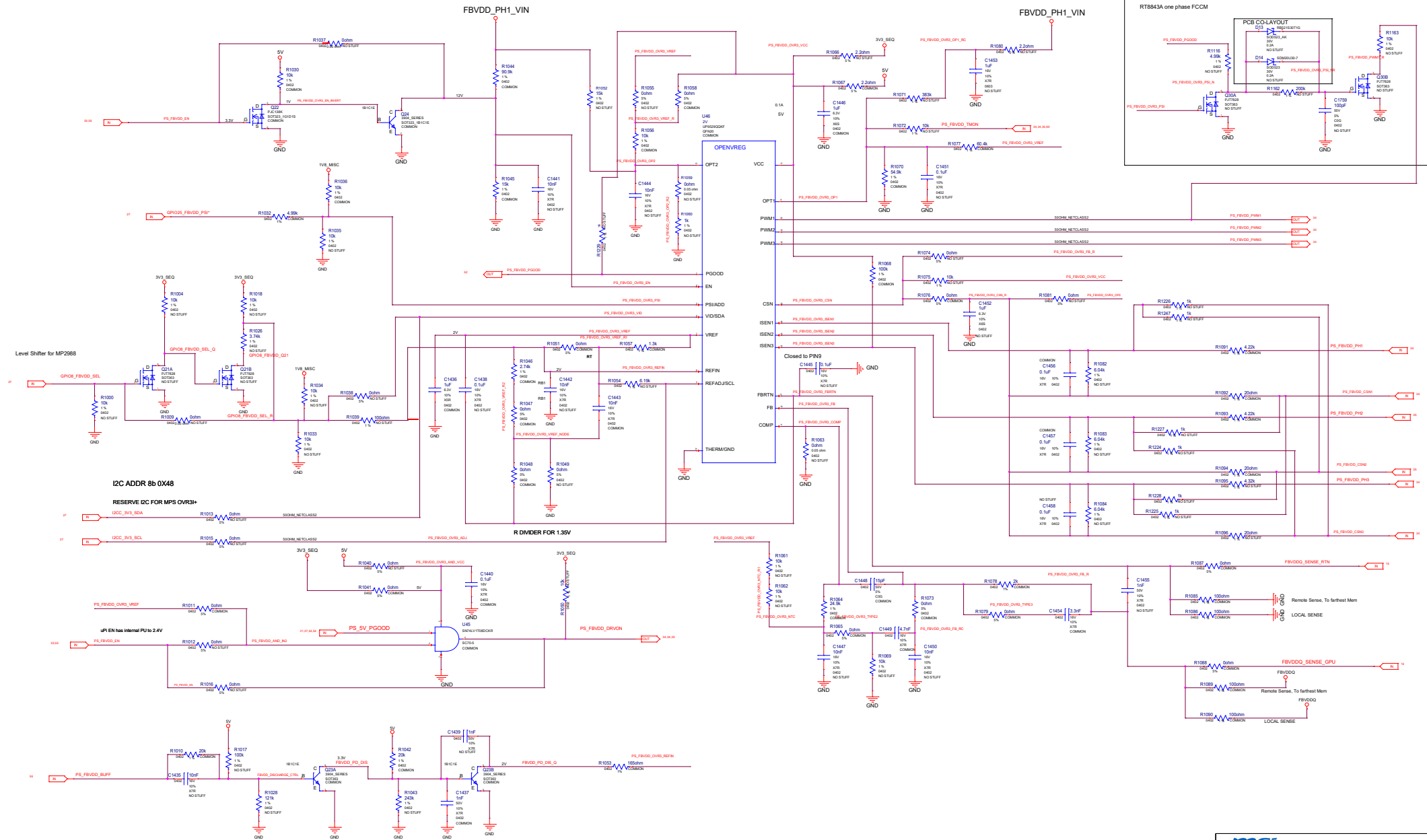
NP1V8



PEX Switcher

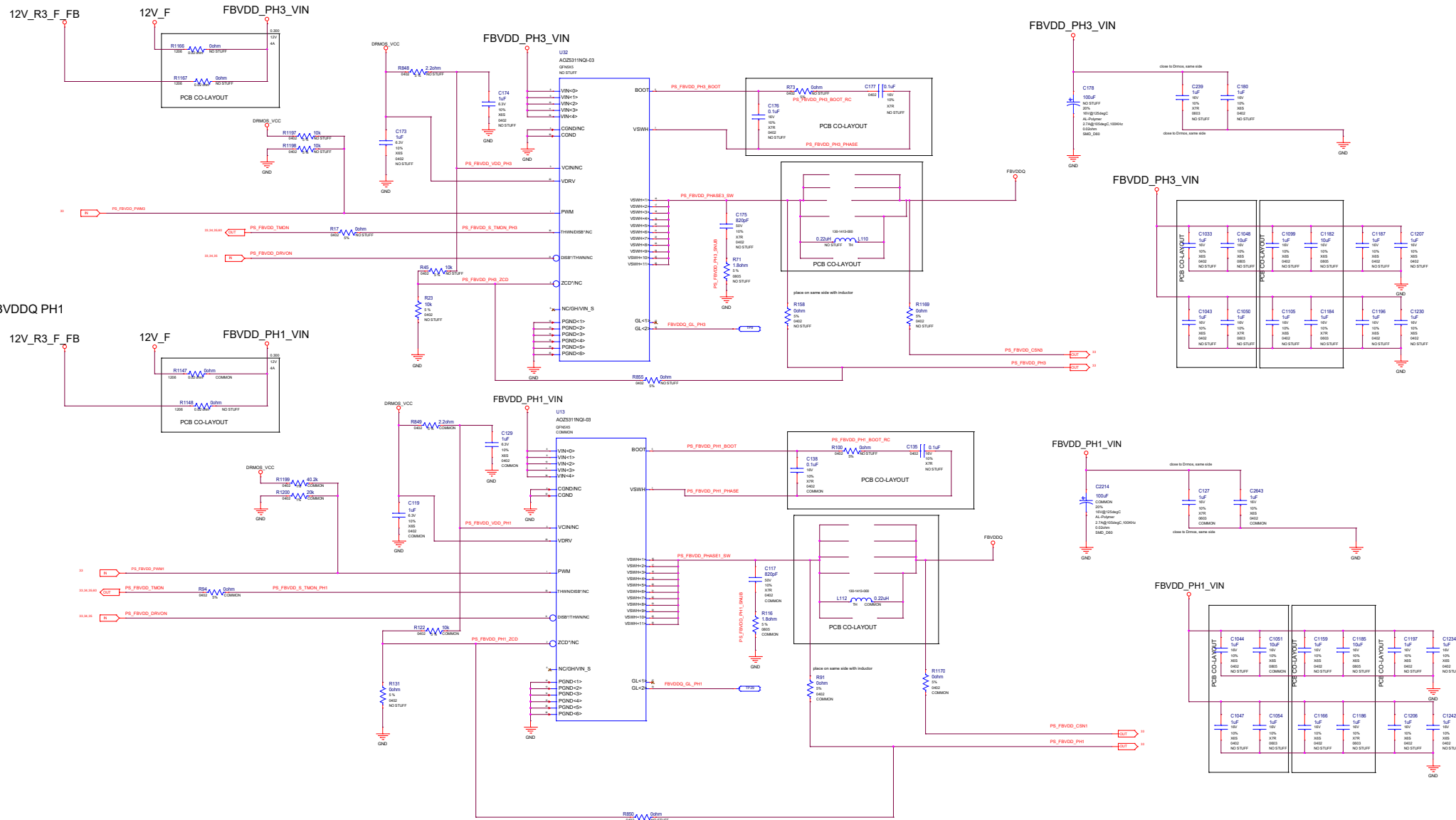


GA 0.95V
 $0.6V \cdot (1 + 10K/16.9K) = 0.955V$
 NP 0.9V
 $0.6V \cdot (1 + 10K/20K) = 0.900V$

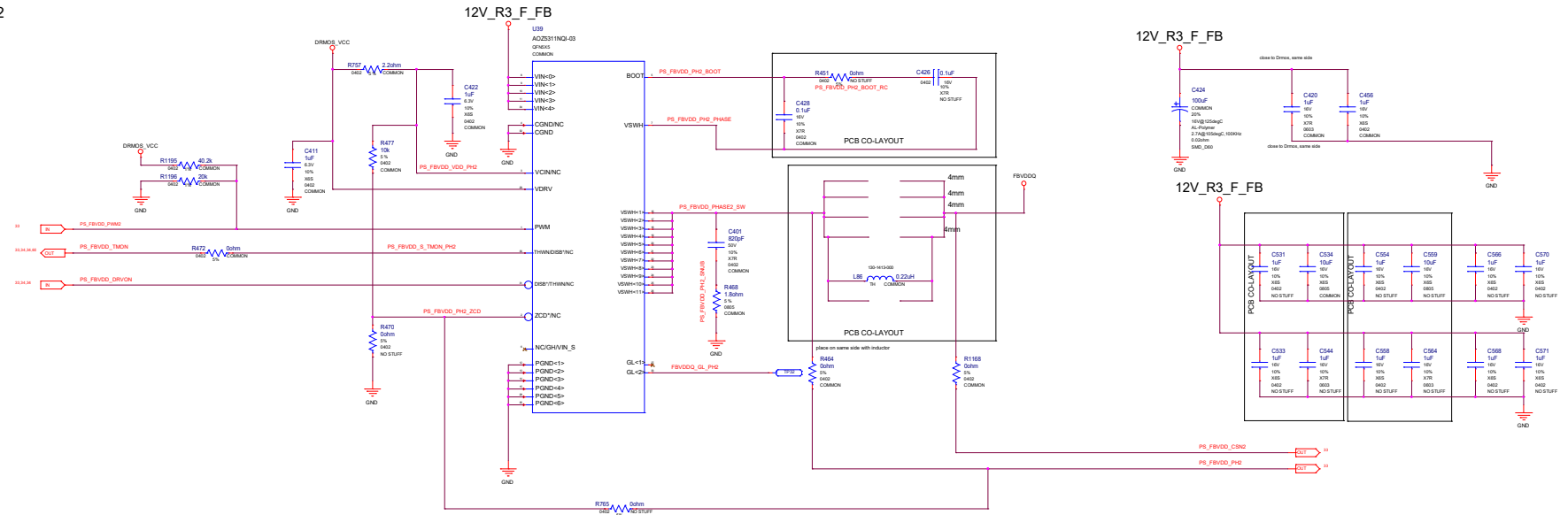


PS: FBVDDQ PH1,PH3

FBVDDQ PH3

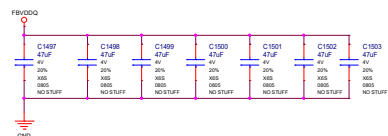


FBVDDQ PH2

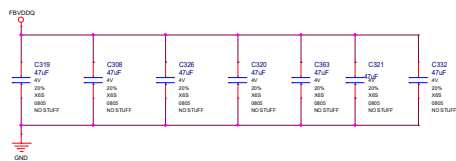


FBVDDQ OUTPUT CAP

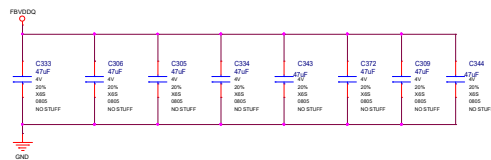
PHASE1



PHASE2

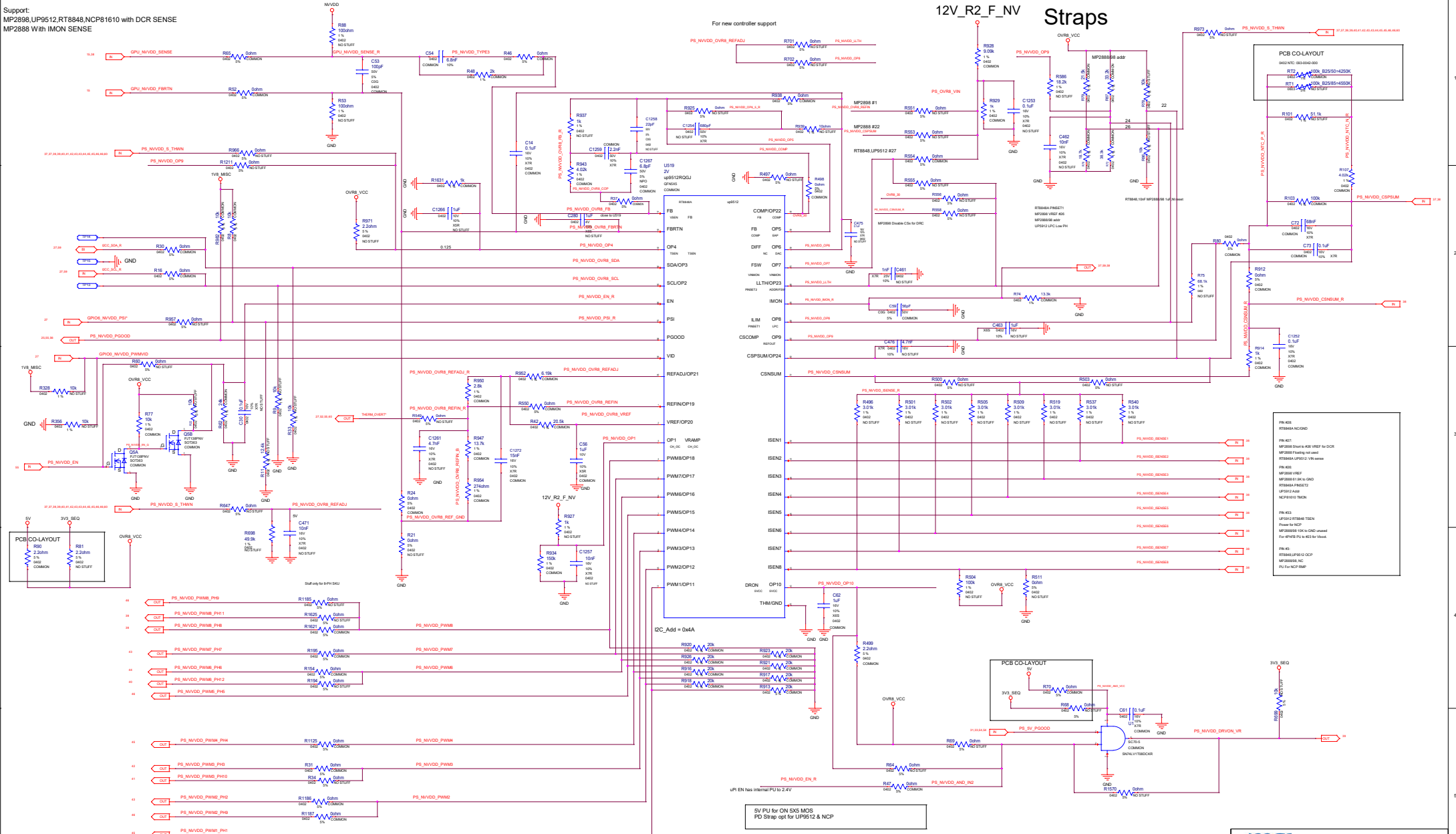


PHASE3

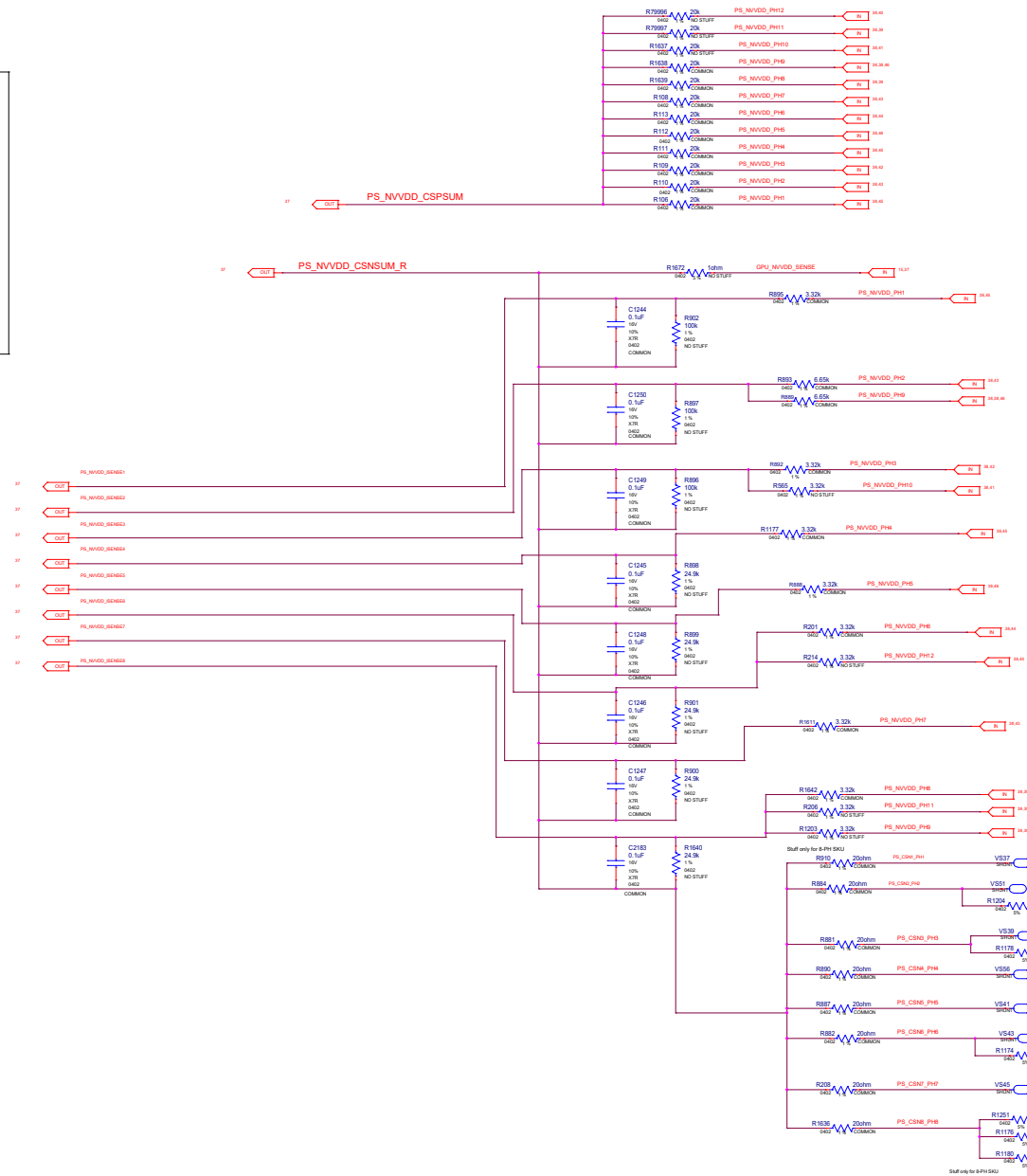
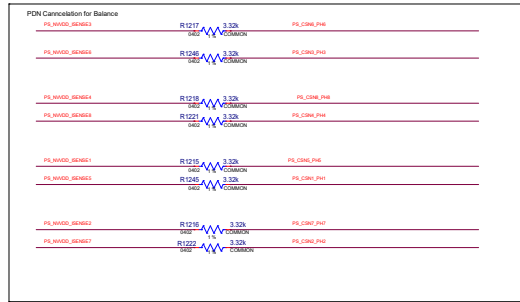


NVDD CTR

Support:
MP2898,UP9512,RT8848,NCP81610 with DCR SENSE
MP2888 With IMON SENSE

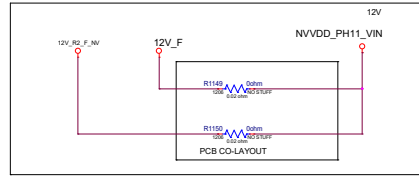


NVVDD PDN Cancellation

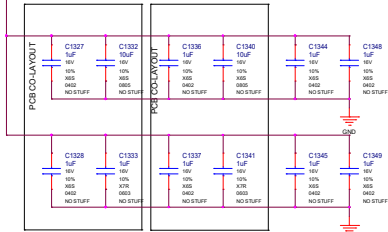


NVVDD PH11 & PH8

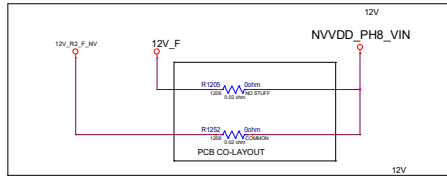
NVVDD PH11(PWM8)



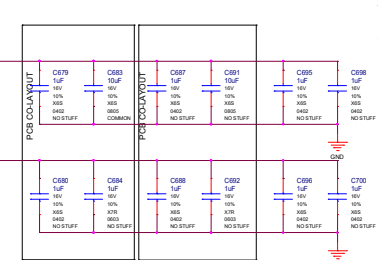
NVVDD_PH11_VIN



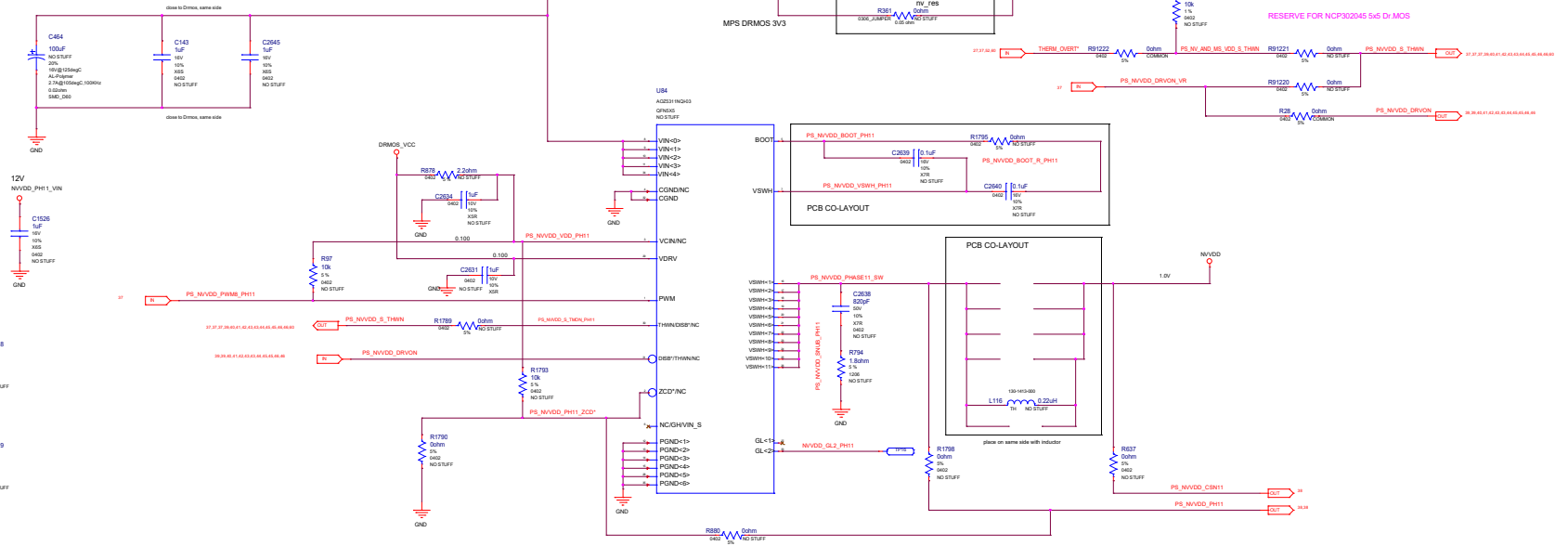
NVVDD PH8(PWM8)



NVVDD_PH8_VIN



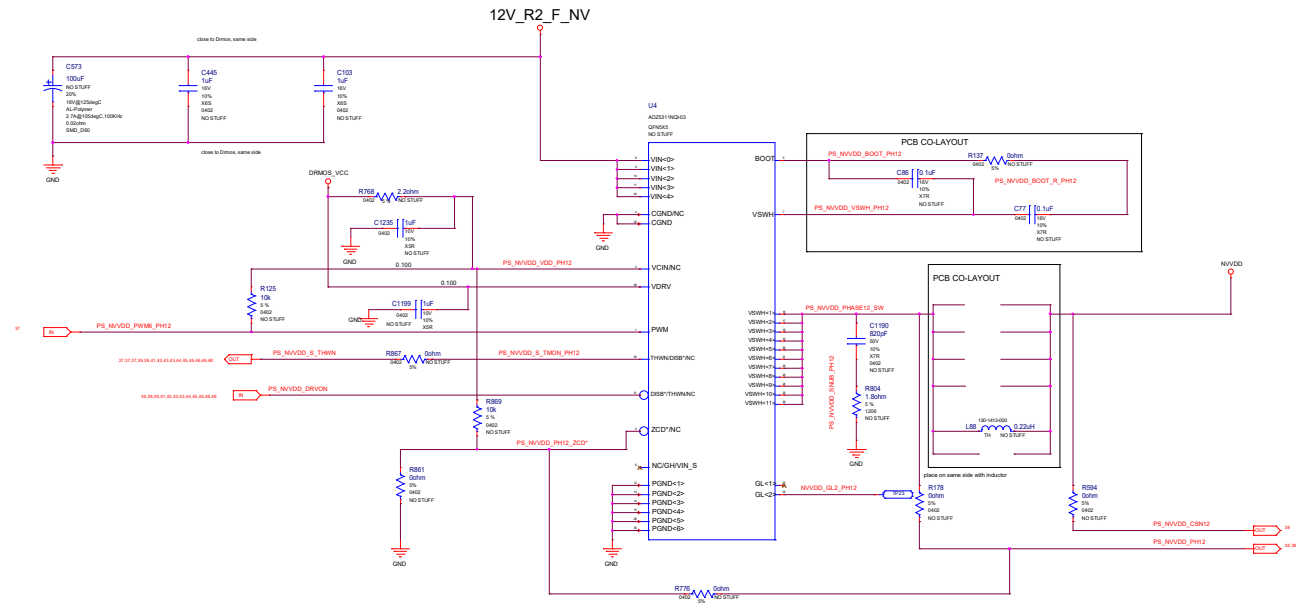
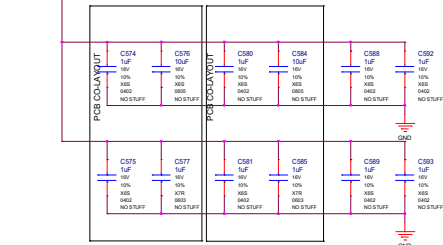
NVVDD_PH11_VIN



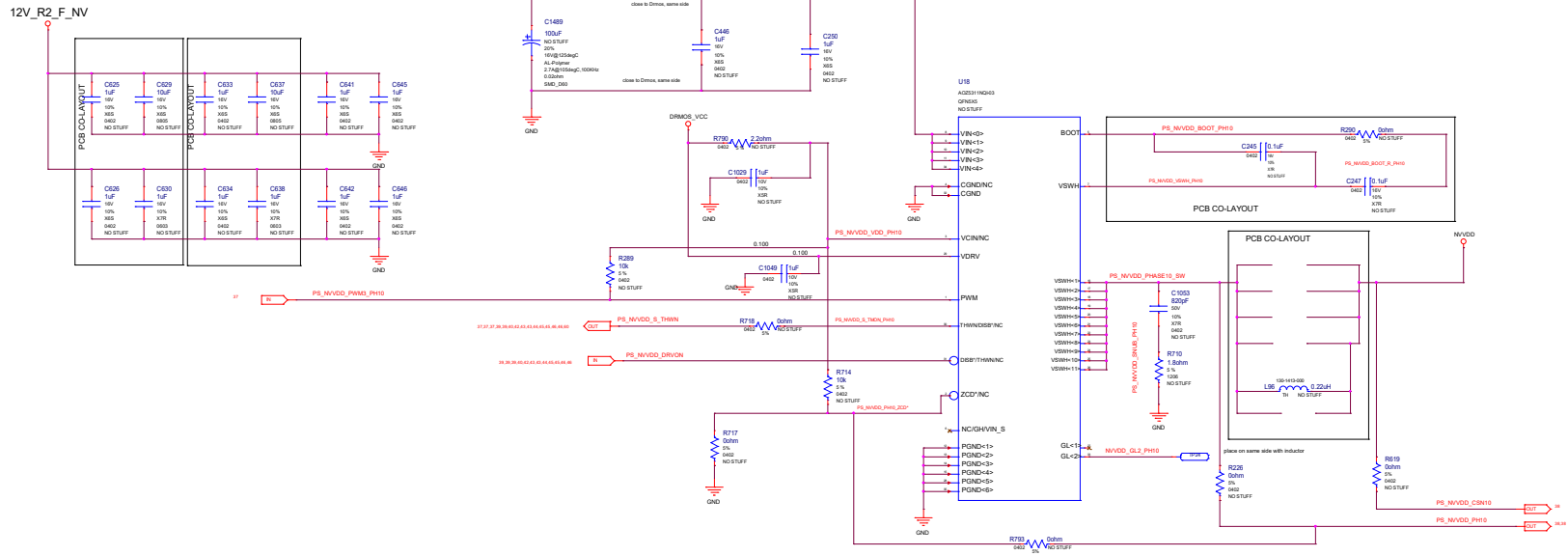
NVVDD PH12

NVVDD PH12(PWM6)

12V_R2_F_NV

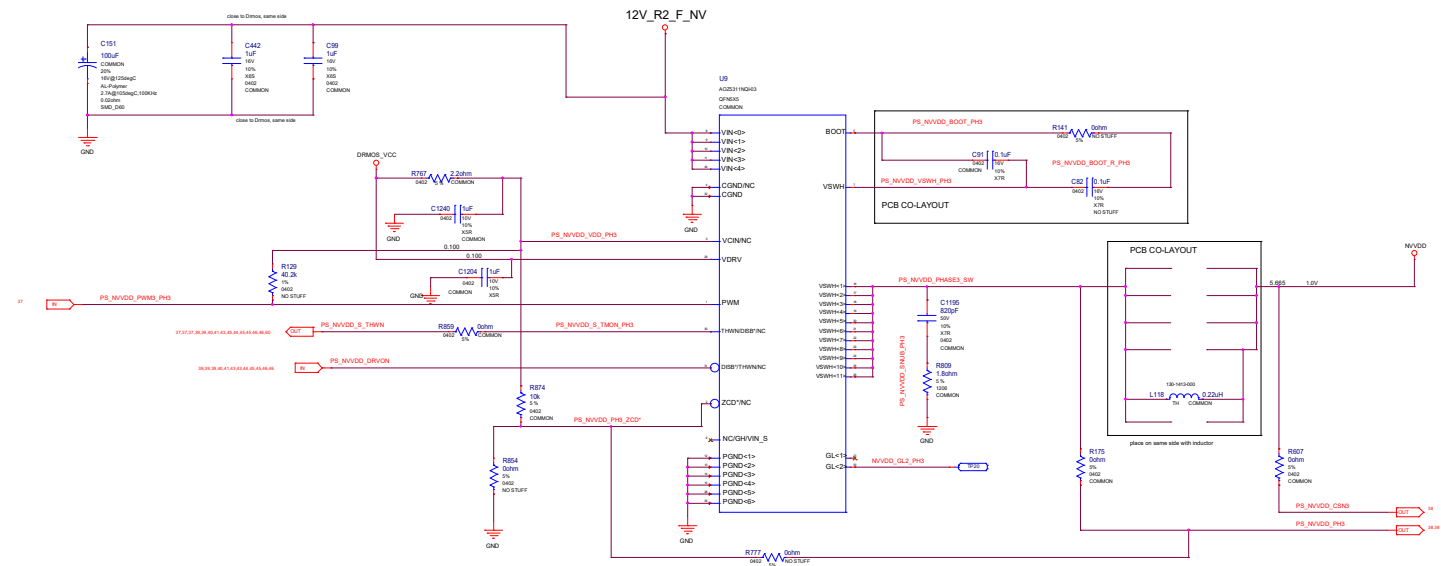
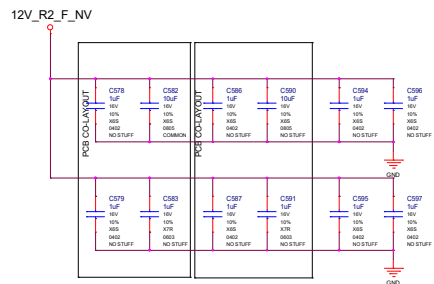


NVVDD PH10
NVVDD PH10(PWM3)



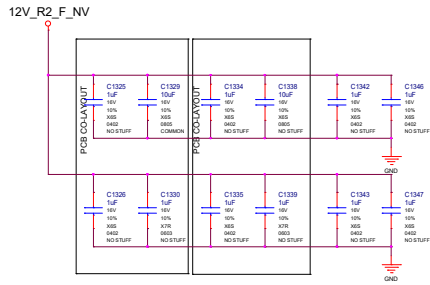
NVVDD PH3

NVVDD PH3(PWM3)

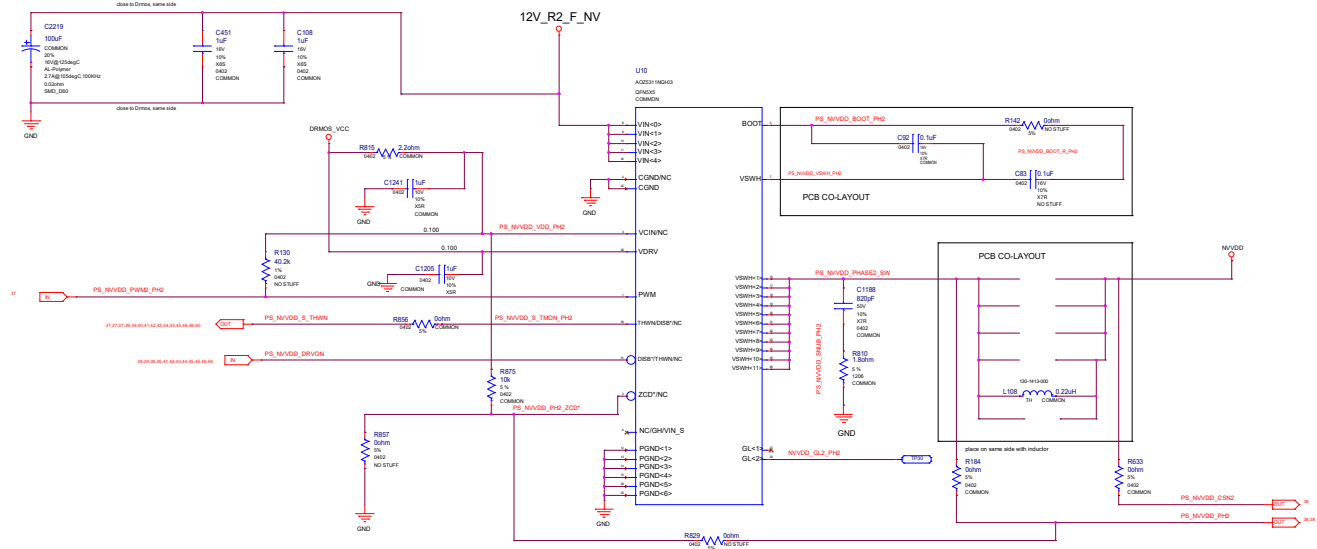
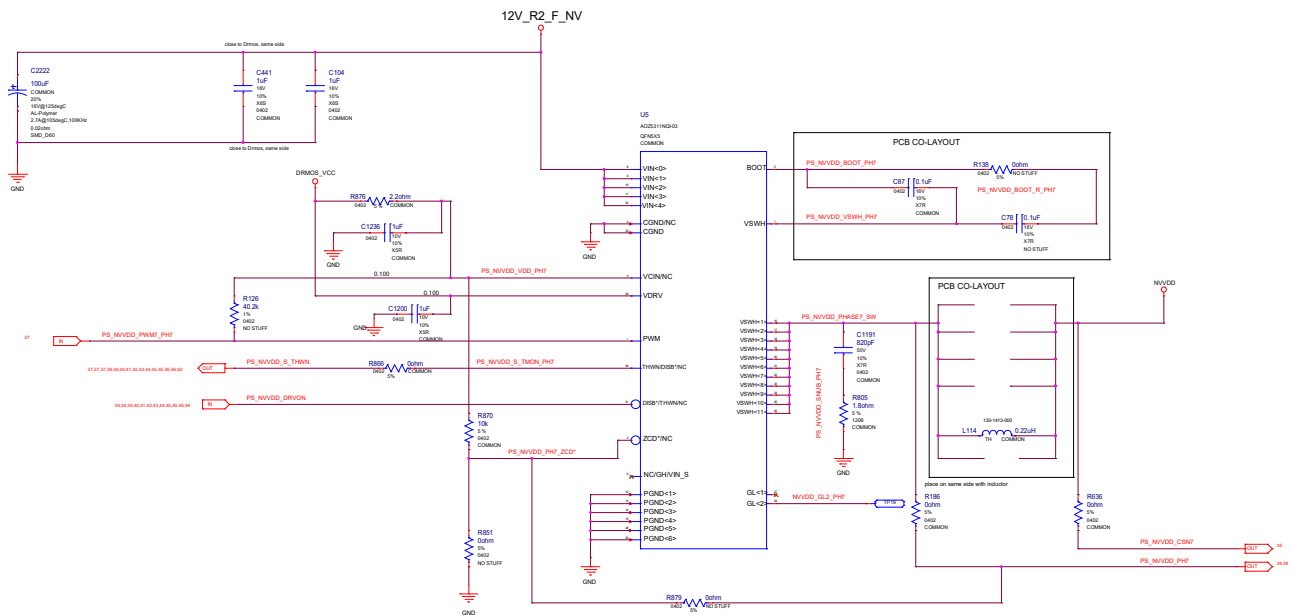
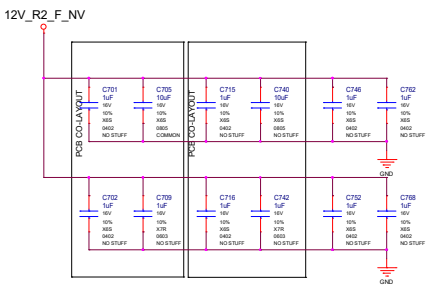


NVVDD PH2 & PH7

NVVDD PH7(PWM7)

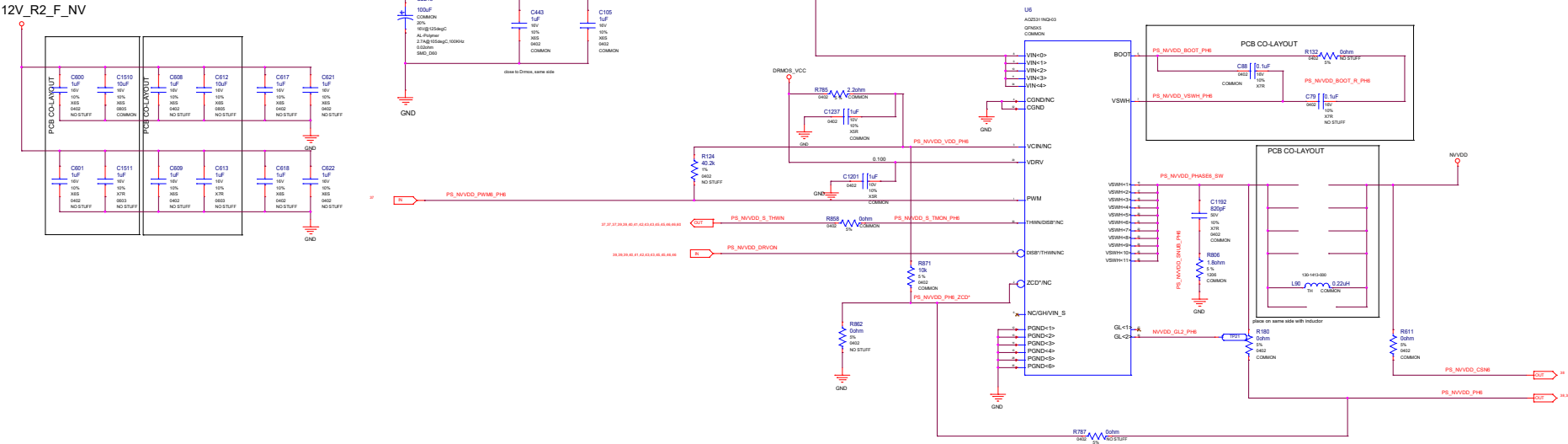



NVVDD PH2(PWM2)



NVVDD PH6

NVVDD PH6(PWM6)

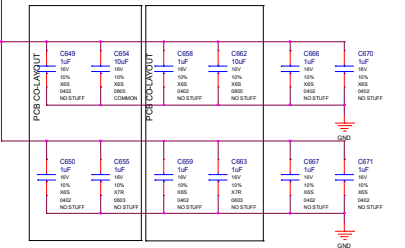


		MICRO-STAR INT'L CO.,LTD.	
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NVDD PH1 & PH4

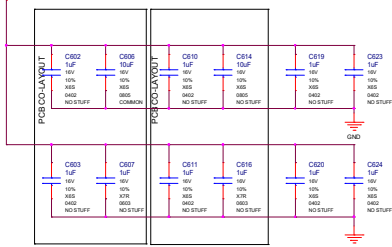
NVDD PH4(PWM4)

12V_R2_F_NV

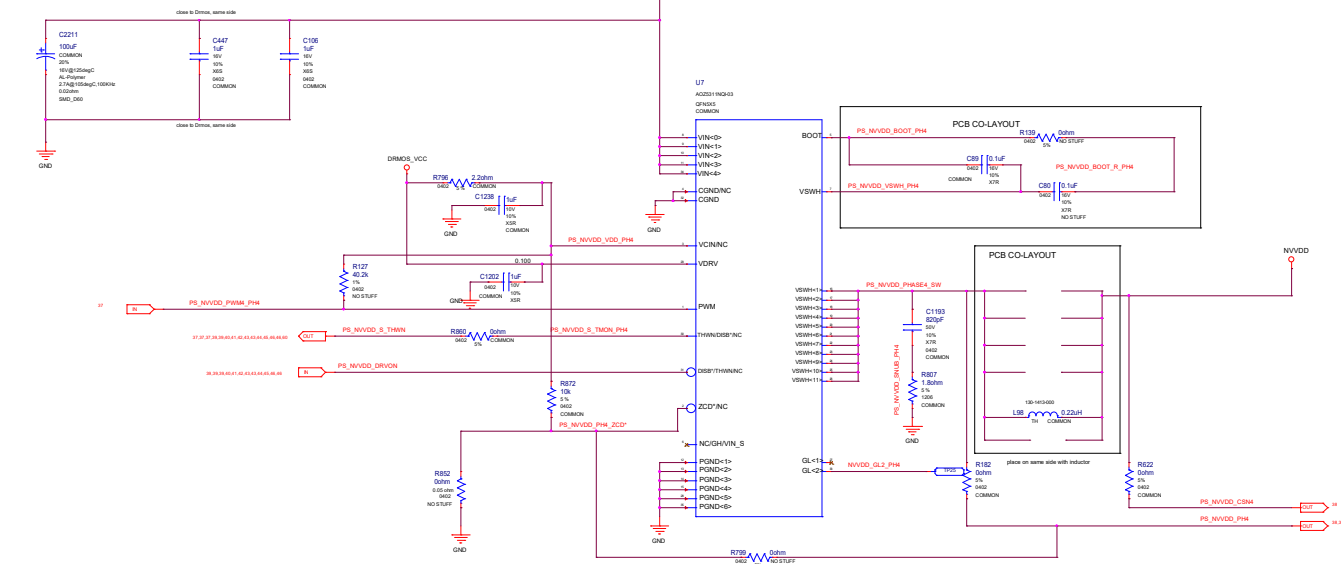


NVDD PH1(PWM1)

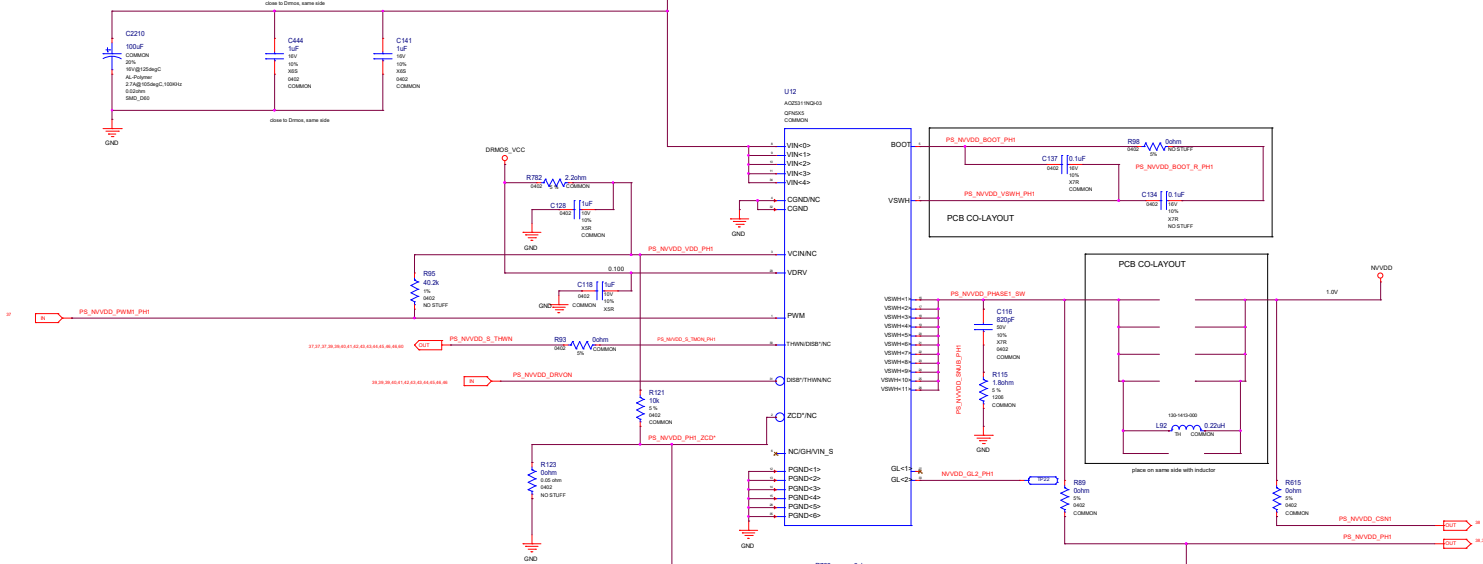
12V_R2_F_NV



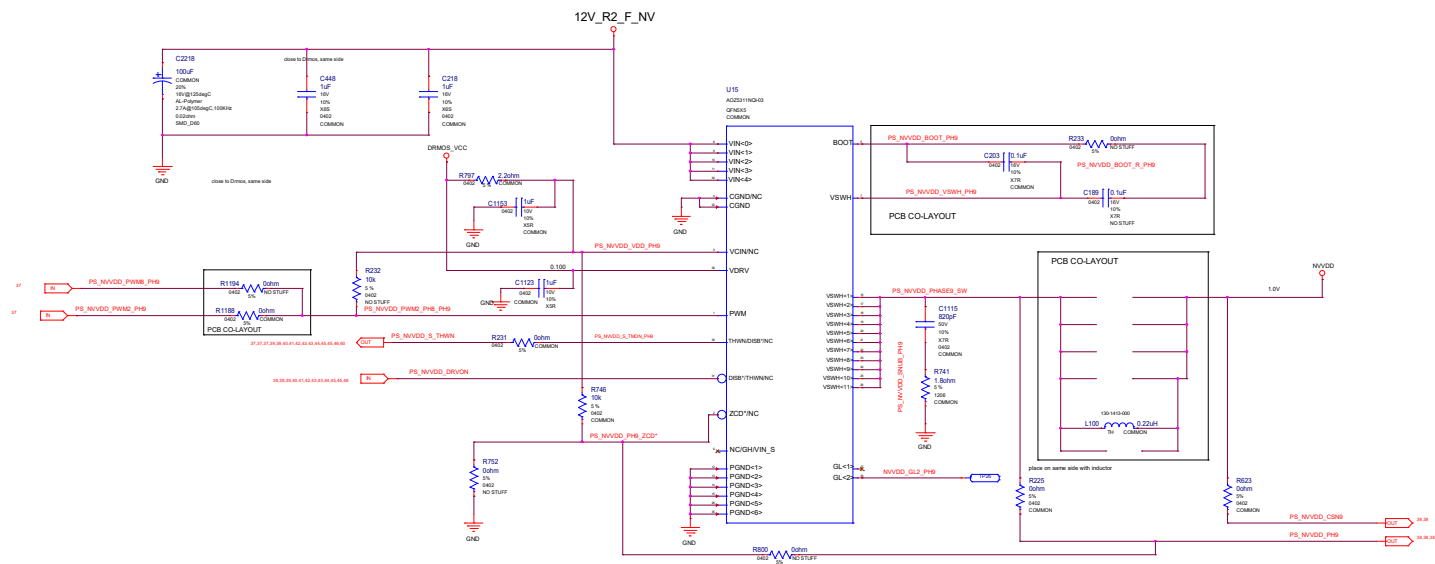
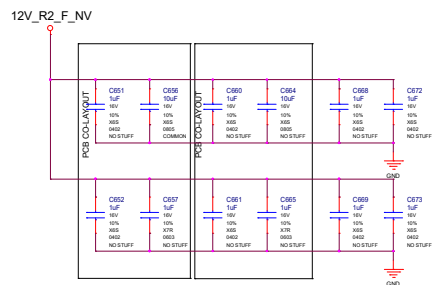
12V_R2_F_NV



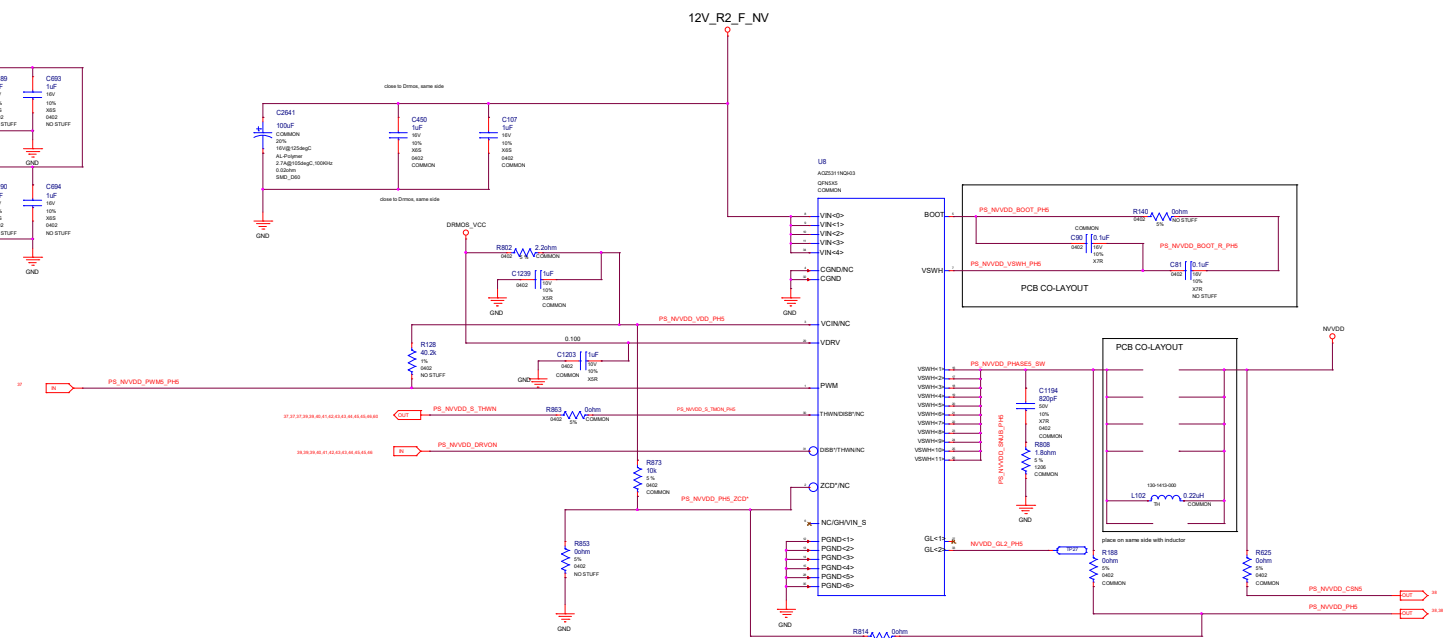
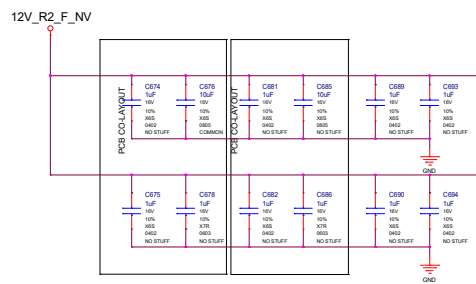
12V_R2_F_NV



NVVDD PH9(PWM2)

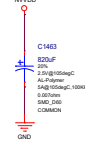
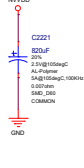
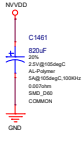


NVVDD PH5(PWM5)

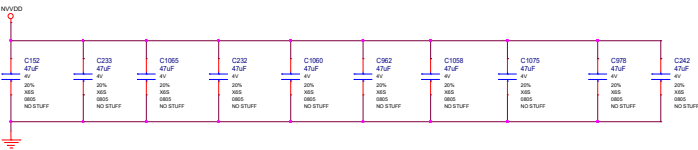
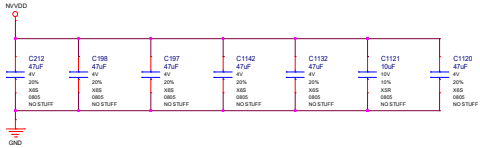
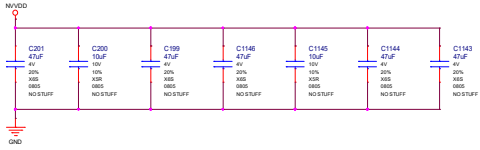
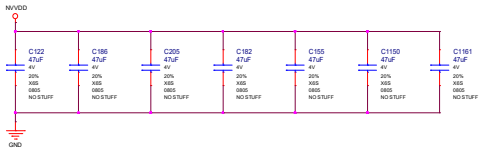


NVVD OUTPUT CAP 1


12xD60



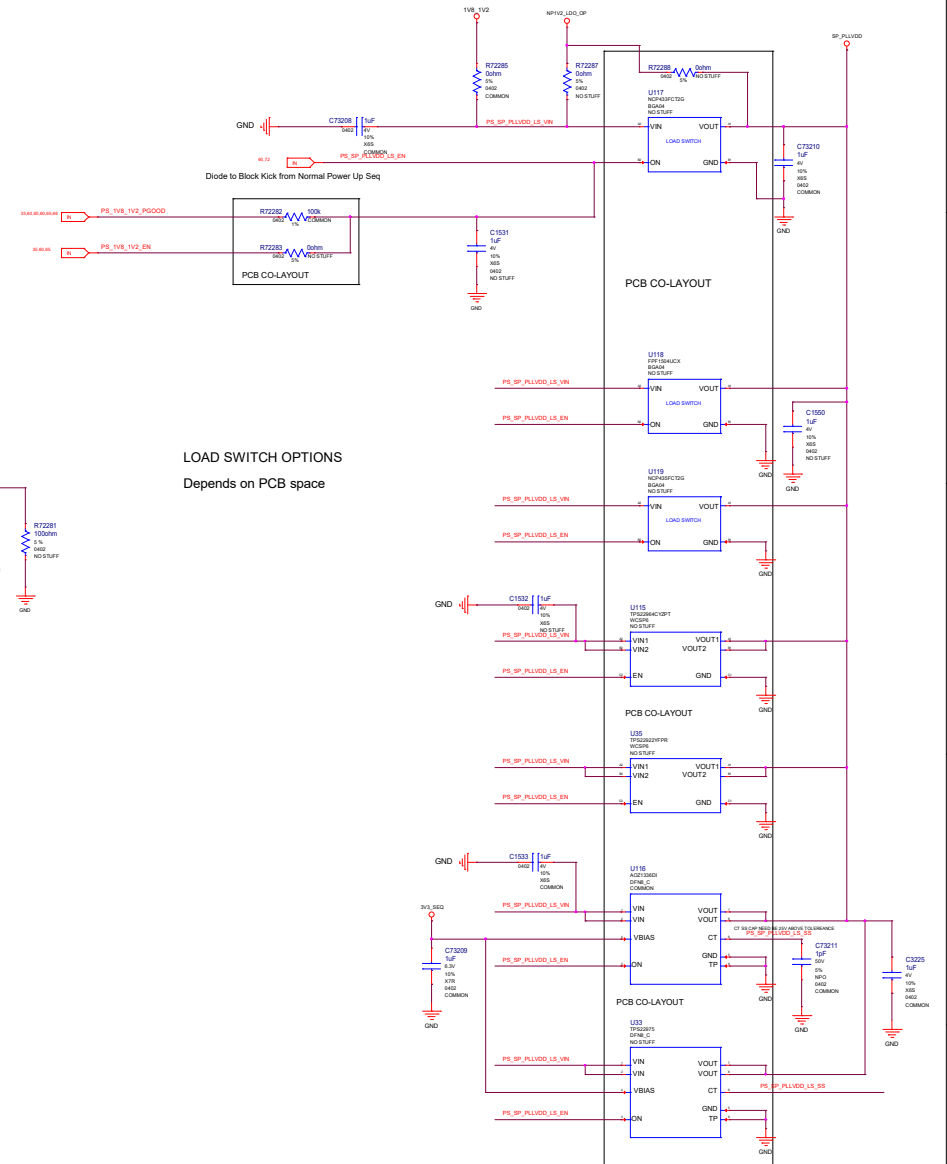
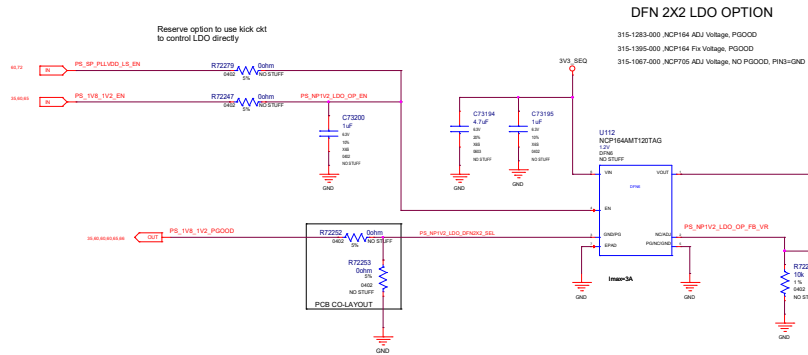
NVDD OUTPUT CAP 2




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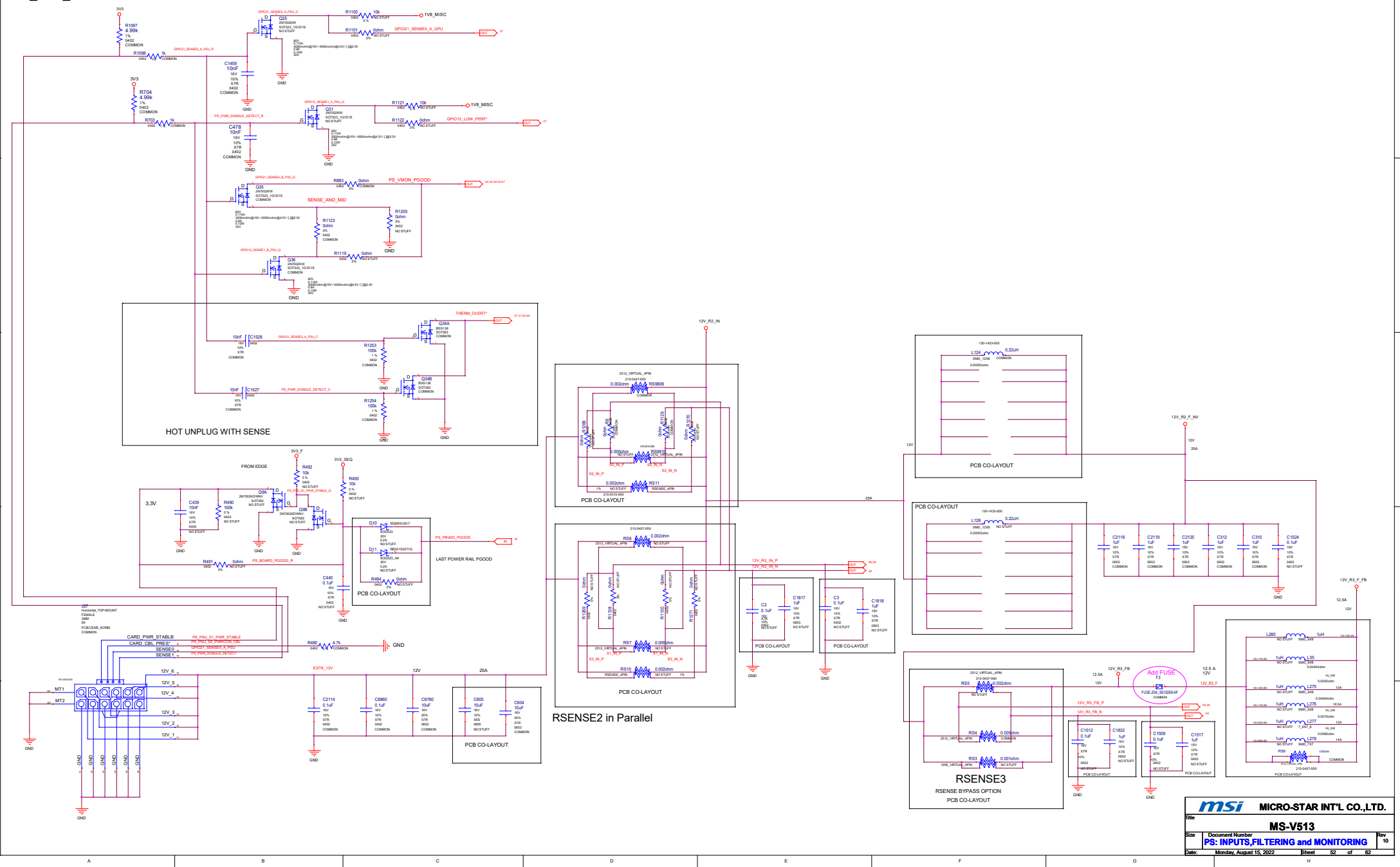
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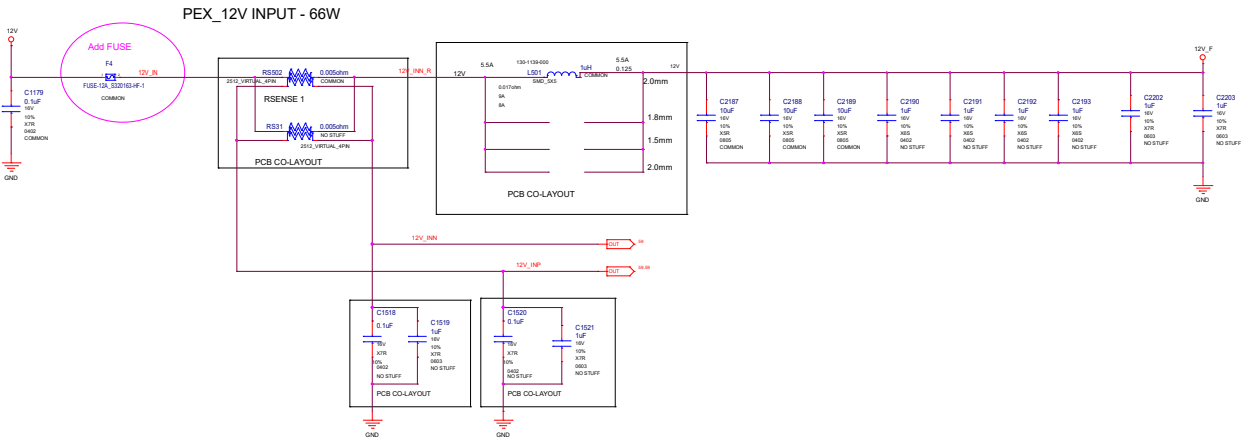
LOAD SWITCH OPTIONS
Depends on PCB space

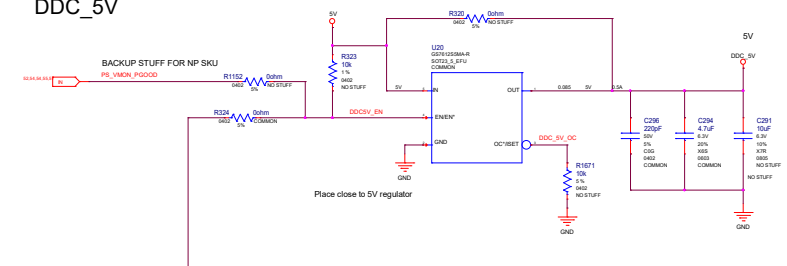
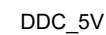
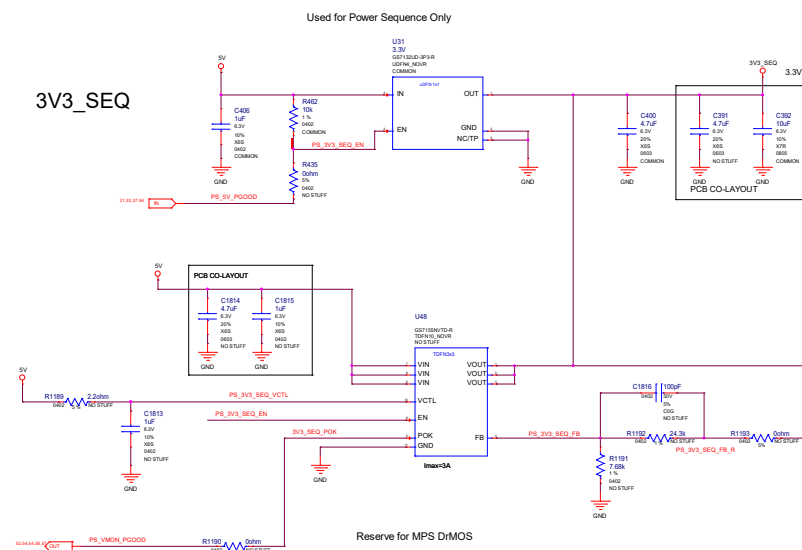
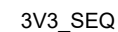
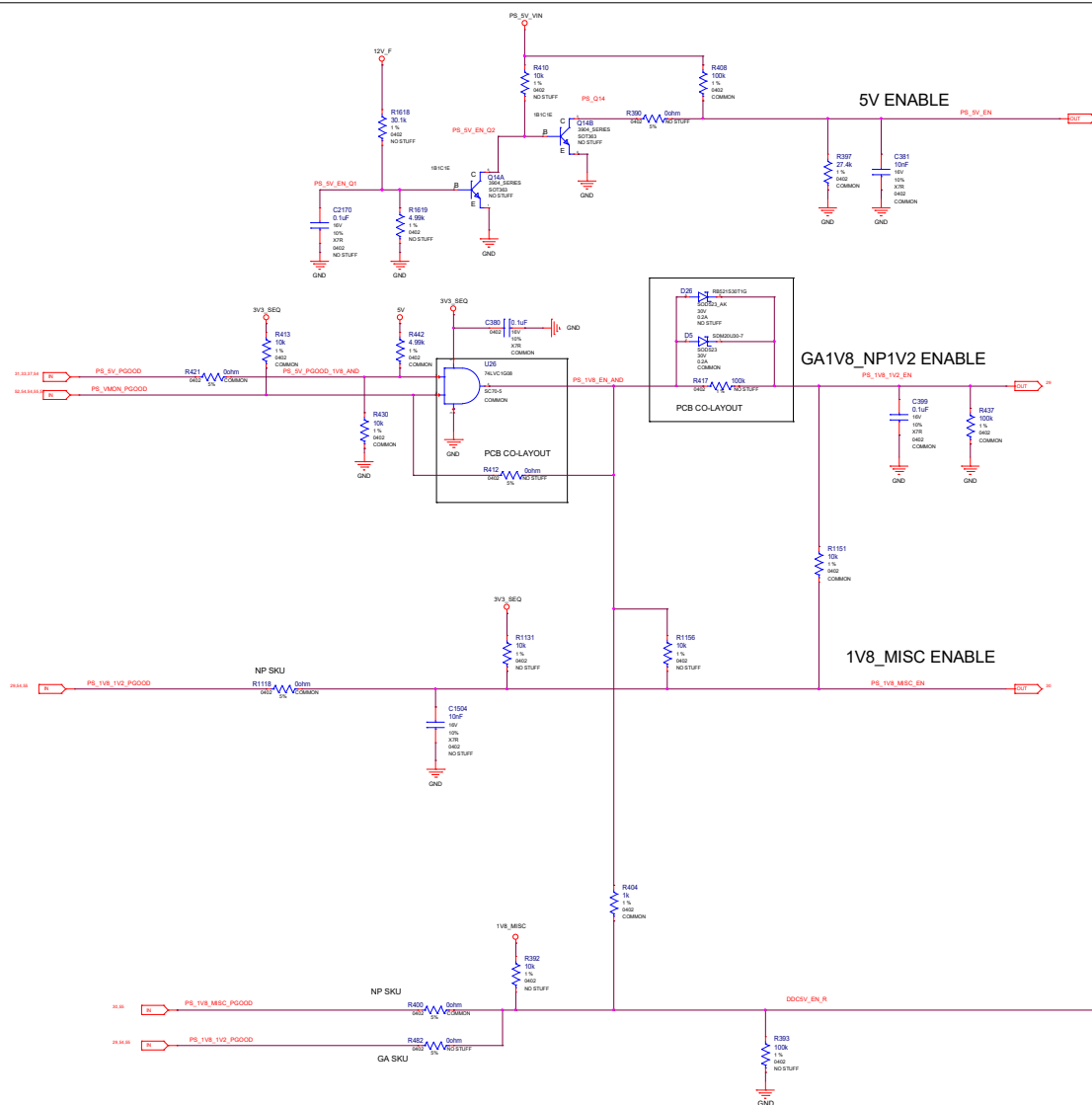
		MICRO-STAR INT'L CO.,LTD.	
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	PS:SP_PLLVDD(LDO_LOADSWITCH)	10	
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12V_EXT_INPUT, FILTERING

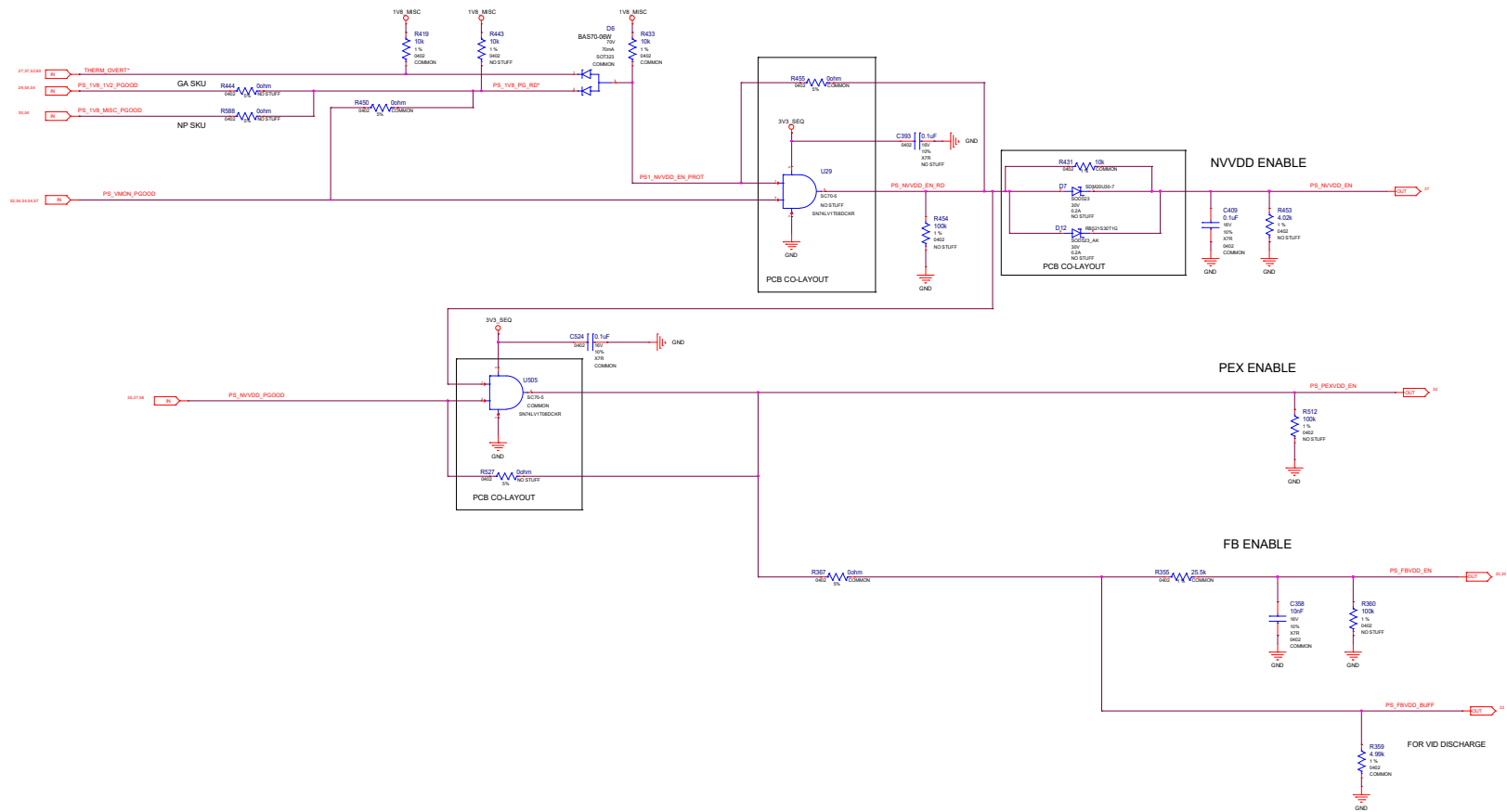


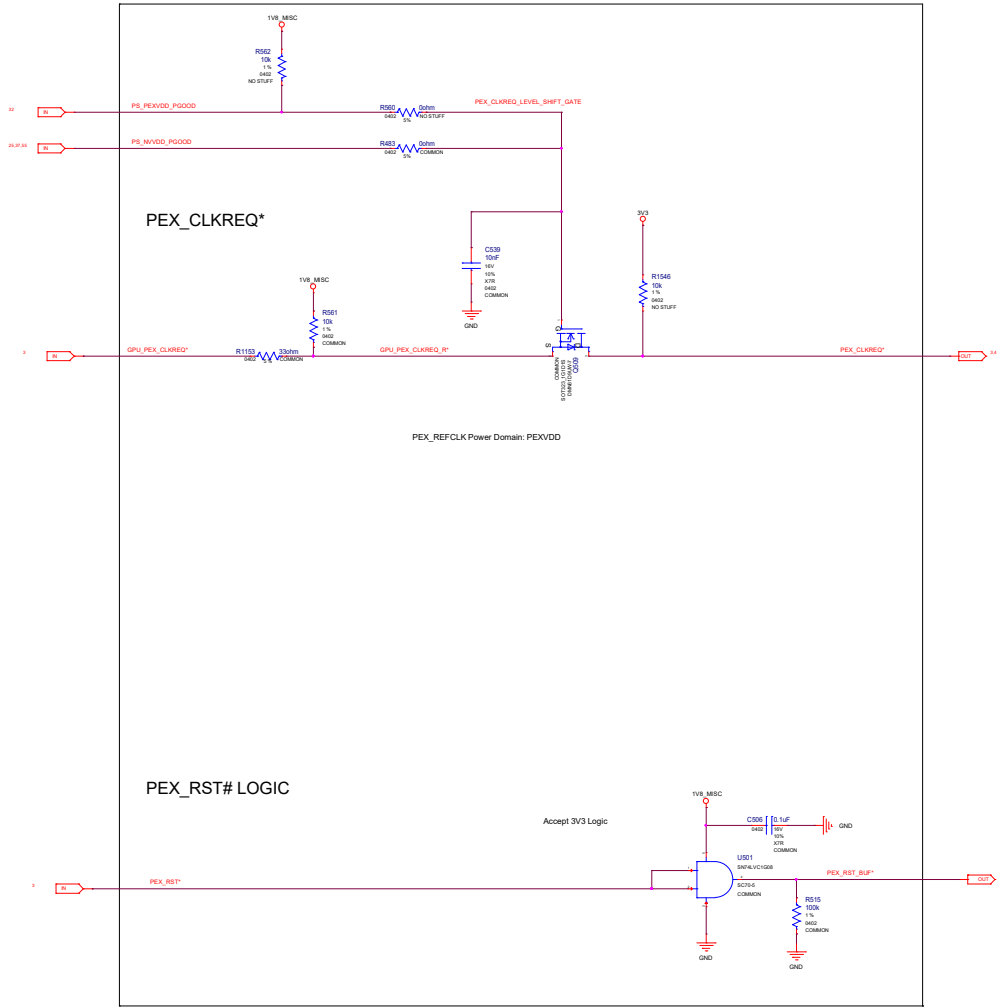
PEX_INPUT & FILTERING, PEX_3V3





SEQ:NVVDD, PEX, FBVDDQ ENABLE

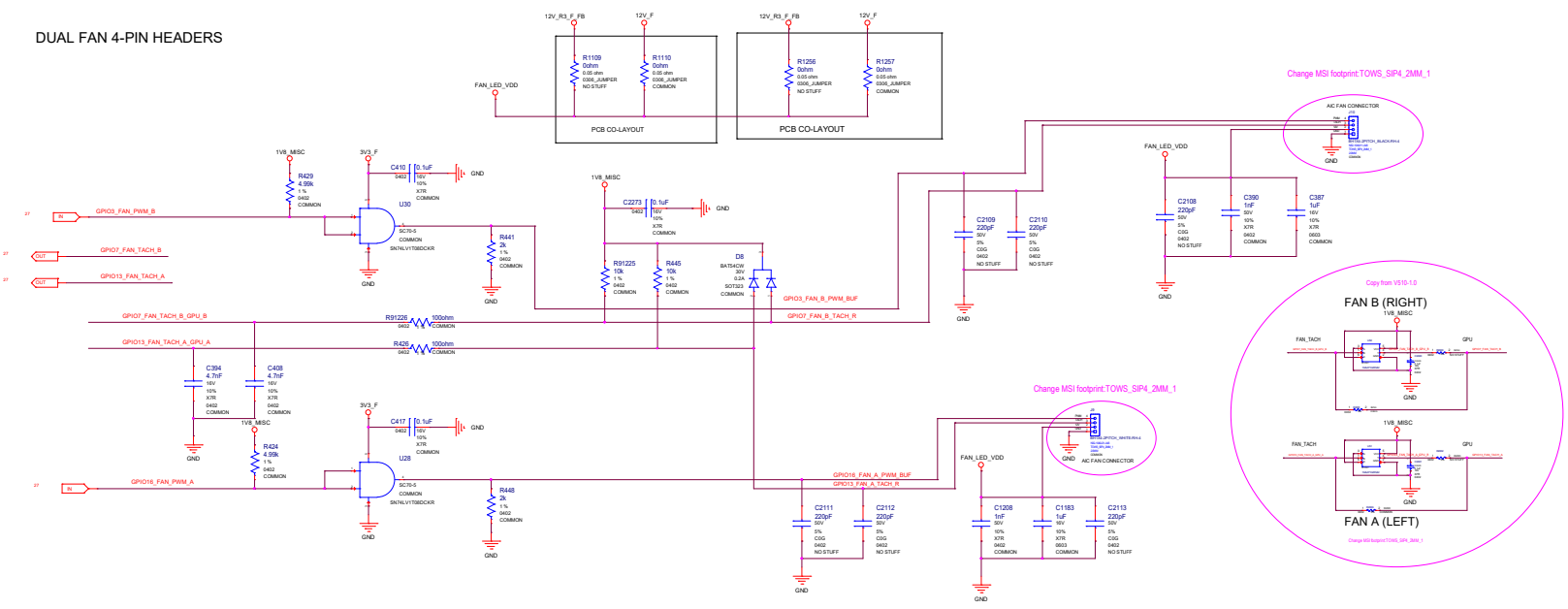


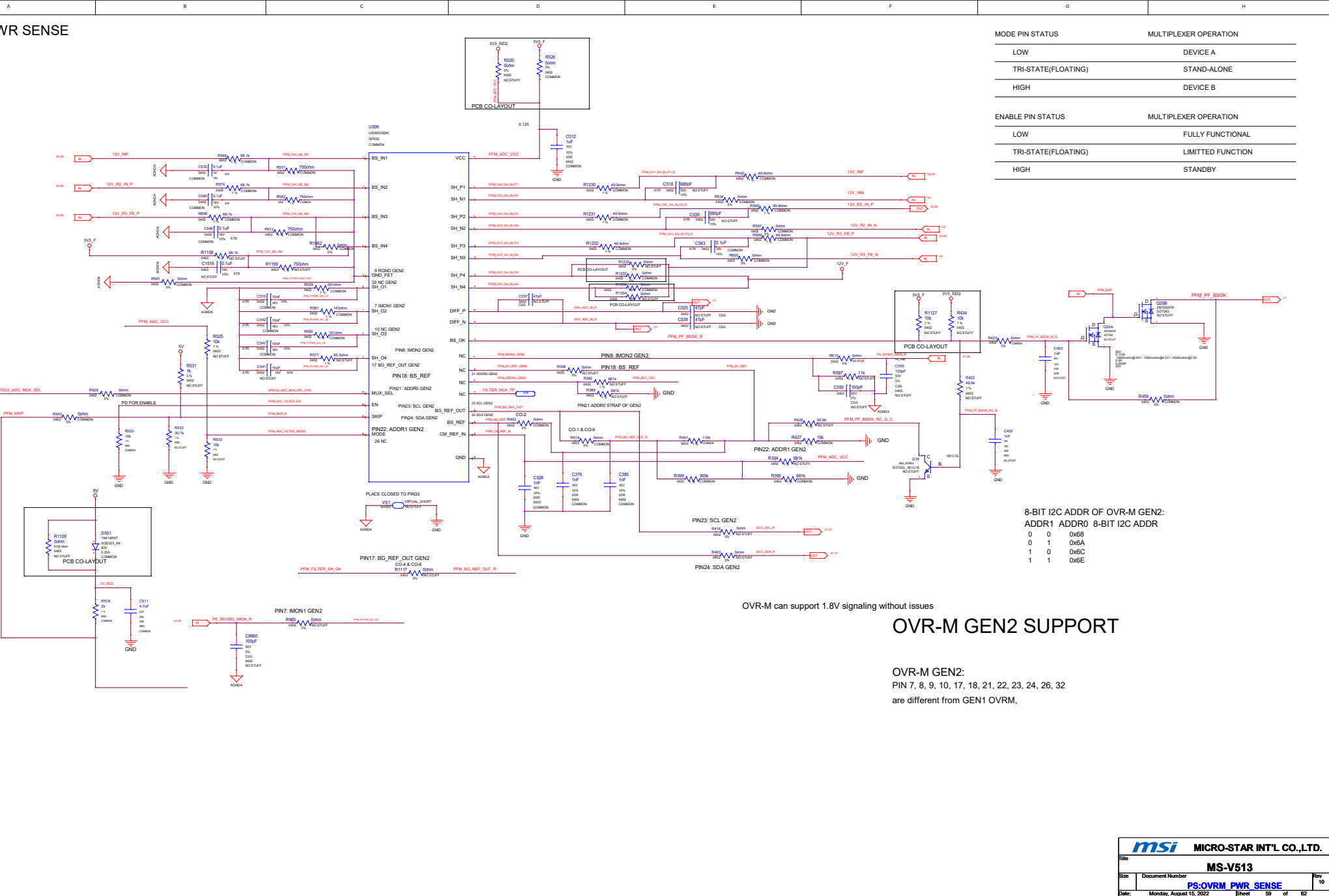


Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIe golden finger
12V	INPUT	Sense the 12V Voltage from PCIe golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC8_FB_EN	INPUT	Indicator for RTD3/GC8 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSKOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)

Remove 2-PIN LED HEADER FOR NORTH LOGO LED (WHITE)

DUAL FAN 4-PIN HEADERS





OVR-M GEN2

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

8-BIT I2C ADDR OF OVR-M GEN2:

ADDR1	ADDR0	8-BIT I2C ADDR
0	0	0x68
0	1	0x6A
1	0	0x6C
1	1	0x6E

OVR-M can support 1.8V signaling without issues

OVR-M GEN2 SUPPORT

OVR-M GEN2:
PIN 7, 8, 9, 10, 17, 18, 21, 22, 23, 24, 26, 32 are different from GEN1 OVRM,

msi MICRO-STAR INT'L CO.,LTD.

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OVR-M GEN2

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

OVR-M GEN2 SUPPORT

OVR-M can support 1.8V signaling without issues

OVR-M GEN2:
PIN 7, 8, 9, 10, 17, 18, 21, 22, 23, 24, 26, 32 are different from GEN1 OVRM,

8-BIT I2C ADDR OF OVR-M GEN2:
ADDR1 ADDR0 8-BIT I2C ADDR

0	0	0x68
0	1	0x6A
1	0	0x6C
1	1	0x6E

MSI MICRO-STAR INT'L CO., LTD.

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OVR-M GEN2

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

8-BIT I2C ADDR OF OVR-M GEN2:

ADDR1	ADDR0	8-BIT I2C ADDR
0	0	0x68
0	1	0x6A
1	0	0x6C
1	1	0x6E

OVR-M can support 1.8V signaling without issues

OVR-M GEN2 SUPPORT

OVR-M GEN2:
PIN 7, 8, 9, 10, 17, 18, 21, 22, 23, 24, 26, 32 are different from GEN1 OVRM,

msi MICRO-STAR INT'L CO.,LTD.

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OVR-M GEN2

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

8-BIT I2C ADDR OF OVR-M GEN2:

ADDR1	ADDR0	8-BIT I2C ADDR
0	0	0x68
0	1	0x6A
1	0	0x6C
1	1	0x6E

OVR-M can support 1.8V signaling without issues

OVR-M GEN2 SUPPORT

OVR-M GEN2:
PIN 7, 8, 9, 10, 17, 18, 21, 22, 23, 24, 26, 32
are different from GEN1 OVRM,

msi MICRO-STAR INT'L CO.,LTD.

File: **MS-V513**

Size: Document Number **PS-OVRM PWR SENSE**

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OVR-M GEN2

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

8-BIT I2C ADDR OF OVR-M GEN2:

ADDR1	ADDR0	8-BIT I2C ADDR
0	0	0x68
0	1	0x6A
1	0	0x6C
1	1	0x6E

OVR-M can support 1.8V signaling without issues

OVR-M GEN2 SUPPORT

OVR-M GEN2:
PIN 7, 8, 9, 10, 17, 18, 21, 22, 23, 24, 26, 32 are different from GEN1 OVRM,

msi MICRO-STAR INT'L CO.,LTD.

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OVR-M GEN2

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

8-BIT I2C ADDR OF OVR-M GEN2:

ADDR1	ADDR0	8-BIT I2C ADDR
0	0	0x68
0	1	0x6A
1	0	0x6C
1	1	0x6E

OVR-M can support 1.8V signaling without issues

OVR-M GEN2 SUPPORT

OVR-M GEN2:
PIN 7, 8, 9, 10, 17, 18, 21, 22, 23, 24, 26, 32 are different from GEN1 OVRM,

msi MICRO-STAR INT'L CO.,LTD.

File: MS-V513

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OVR-M GEN2

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

8-BIT I2C ADDR OF OVR-M GEN2:

ADDR1	ADDR0	8-BIT I2C ADDR
0	0	0x68
0	1	0x6A
1	0	0x6C
1	1	0x6E

OVR-M can support 1.8V signaling without issues

OVR-M GEN2 SUPPORT

OVR-M GEN2:
PIN 7, 8, 9, 10, 17, 18, 21, 22, 23, 24, 26, 32 are different from GEN1 OVRM,

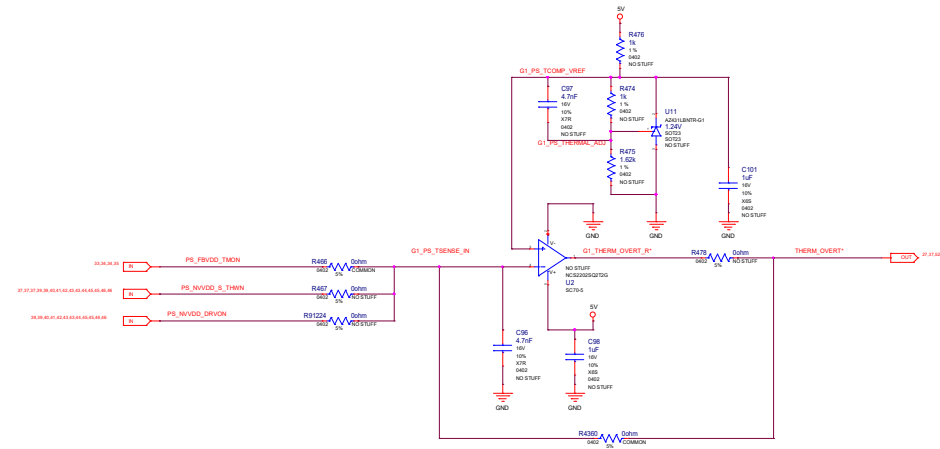
msi MICRO-STAR INT'L CO., LTD.

File: MS-V513

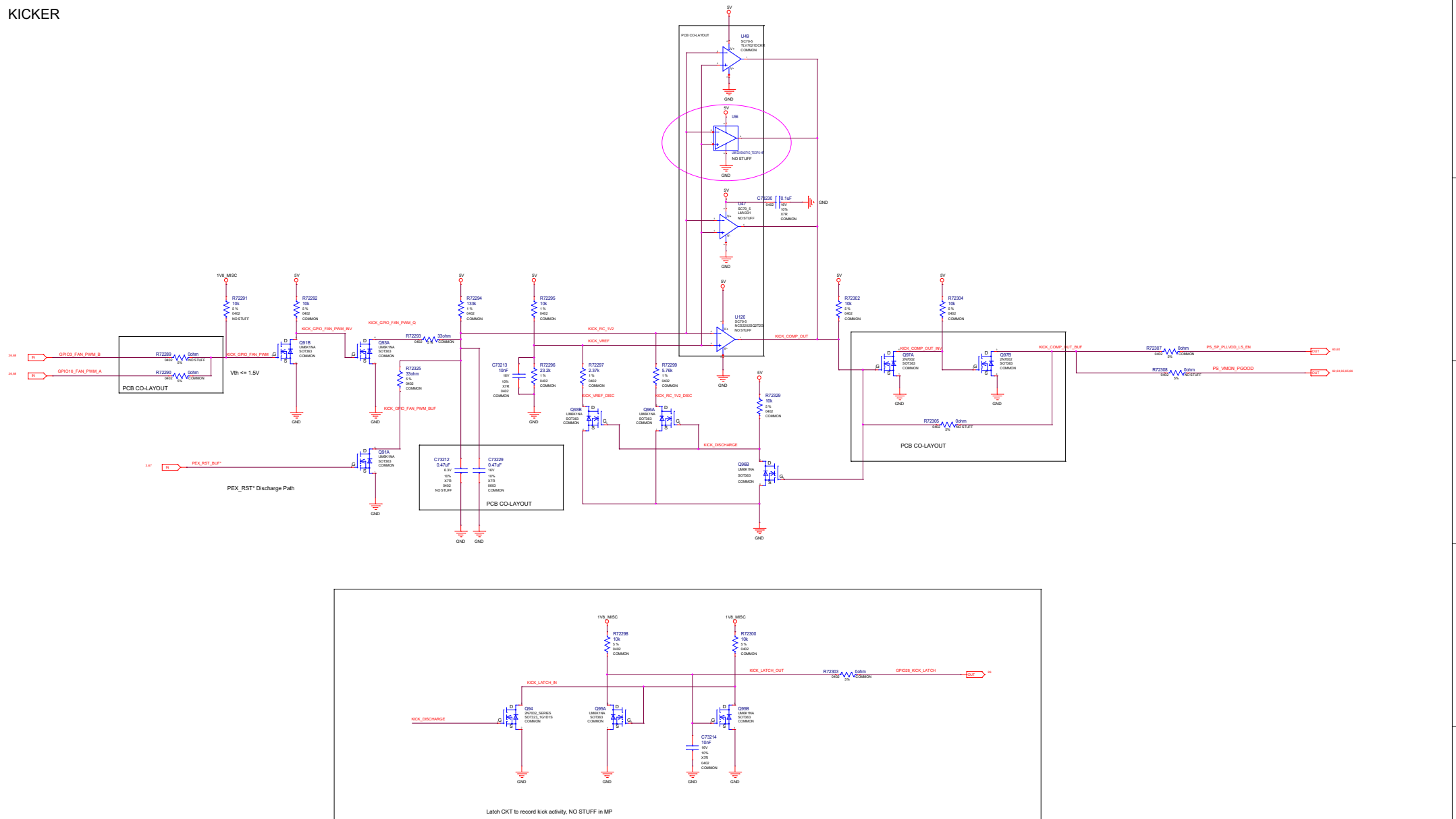
Size: Document Number PS-OVRM PWR SENSE Rev 10

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VR THERMAL PROTECTION



KICKER



MOUNTING HOLES

